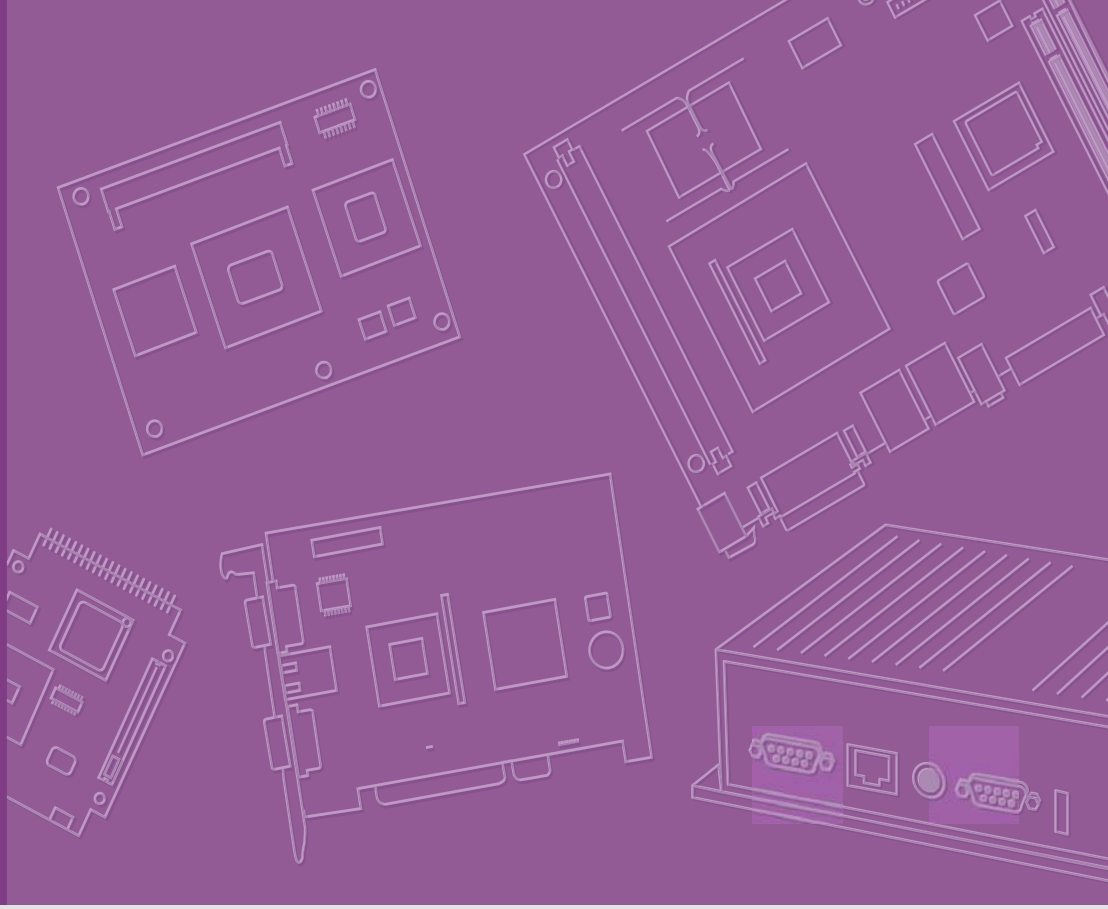

User Manual

POD-6552 A2

Trusted ePlatform Services

ADVANTECH

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FCC

This device complies with the requirements in part 15 of the FCC rules: Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this device in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his/her own expense. The user is advised that any equipment changes or modifications not expressly approved by the party responsible for compliance would void the compliance to FCC regulations and therefore, the user's authority to operate the equipment.

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Additional Information and Assistance

1. Visit the Advantech web site at http://www.advantech.com/ where you can find the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Packing List

Before installation, please ensure the following items have been shipped:

- 1 POD-6552 A2 SBC
- 1 Startup manual
- 1 Utility CD
- 1 Power Cable 12P/Big 4Px2, 10 cm 1700006196
- 1 mini jumper pack 9689000002

Ordering information

Model Number	Description
POD-6552L-00A2E	Intel Socket 479 w/CRT/LVDS/TV out/4 COM/Audio/CF/16 USB
POD-6552L-M0A2E	Intel C-M 600 M w/CRT/LVDS/TV out/4 COM/Audio/CF/16 USB
POD-6552L-S0A2E	Intel C-M 1.0 G w/CRT/LVDS/TV out/4 COM/Audio/CF/16 USB

Part No.	POD-6552L-00A2E	POD-6552L-M0A2E	POD-6225L-S0A2E
CPU	Socket 479	Celeron M 600 MHz	Celeron M 1.0 GHz
La Cache	-	512 KB	-
CRT	Yes	Yes	Yes
LVDS	18-bit	18-bit	18-bit
TV Out	Yes	Yes	Yes
10/100	1	1	1
Audio	Yes	Yes	Yes
USB 2.0	6	6	6
RS-232	3	3	3
RS-232/422/485	1	1	1
LPT/FDD/KB/MS	Yes	Yes	Yes
CF	Yes	Yes	Yes
PCI Slot	2	2	2
Thermal Solution	Active	Passive	Passive
Operating Temp.	0 ~ 60° C	0 ~ 60° C	0 ~ 60° C

Optional accessories

Part Number	Description
PCM-10586-6552E	Wiring kit for POD-6552 Series
1700001112	ATX power cable
PCM-110-00A3E	1-slot PCI riser card for 5.25" biscuits
PCM-120-00A3E	2-slot PCI riser card for 5.25" biscuits
CF-HDD-ADP	CompactFlash 50-pin to IDE 44-pin adapter

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Chapter 1

General Introduction

This chapter gives background information on POD-6552 A2.

Sections include:

- **Introduction**
- **Specifications**

1.1 Introduction

- Intel® Celeron® M processor with fanless design
- EBX form factor standard, supports PC/104
- One SODIMM up to 1 G DDR 200/266 MHz
- Dual Display (CRT + LVDS, CRT + TV-Out, LVDS +TV-Out)
- Supports up to 400 MHz Processor Side Bus
- Supports up to 266 MHz DDR SODIMM
- Supports six USB 2.0 ports

1.2 Product Specifications

POD-6552 A2 is reversion from A1. For system I/O ports, PCM-6552 A2 add Super IO runtime register and change COM2 address from 2F8 ~ 2FF to 2E0~2E7. The list is as follow.

	A1	A2
COM2	2F8 - 2FF	2E0 - 2E7
Super IO runtime register :	No	800h - 87Fh

1.2.1 General

- **CPU:** On board type: C-M 600MHz/ 1.0G Hz,
  Socket type: Socket 479
- **L2 Cache:** On board type: 512K L2 (C-M 600) / 0L2 (C-M 1G),
  Socket type: Depend on CPU
- **System Chipset:** Intel 852GM + ICH4
- **BIOS:** Award 4Mb LPC BIOS
- System Memory: One SODIMM up to 1GB DDR 200/266MHz
- **Power Management:** APM1.2, ACPI support
- **Watchdog Timer:** 255-level interval timer, setup by software, Super I/O integrated, SMSC Controller
- **Expansion Interface:** Supports PC-104, ISA slot, PCI slot x2
- **Battery:** Lithium 3 V / 196 mAH

1.2.2 I/O

- **I/O Interface:**
  - 1 x EIDE (PIO/DMA-33), 2 x Floppy, 1 x K/B,
  - 1 x Mouse, 3 x RS232, 1 x RS232/422/485, 1 x LPT
- **USB:** 6 x USB 2.0 compliant ports
- **Audio:** AC97, Line-in, Line-out, Mic-in, speaker out (R/L)
- **IrDA -:** 115 kbps (optional by request)

1.2.3 Ethernet

- **Chipset:** 1 x Realtek RTL8139DL
- **Speed:** 10/100Mbps
- **Interface:** 1 x RJ45
- **Standard:** IEEE 802.3u 100Base-T

1.2.4 Display

- **Controller:** Intel 910GMLE
- **VRAM:** Optimized Shared Memory Architecture up to 64 MB system memory
- **LVDS LCD:** 18 bit LVDS (Optional for 2 channel 2 x 18bit LVDS)
- **DSTN:** Yes (Optional by request)
- **TTL:** 18-bit TTL
- **VGA:** 1024 x 768 @ 16 bpp (85 Hz)
- **Dual Independent Display:** CRT + LVDS, CRT + TV-Out, LVDS + TV-Out

1.3 Chipset

1.3.1 Functional Spec.

1.3.1.1 Processor

Processor	■ On board Intel Celeron M processor 600 MHz / 1.0 GHz (0L2) ■ Socket 479 for Celeron® M and Pentium® M CPU (Optional) ■ 400 MHz FSB Support

1.3.1.2 Chipset (852GM)

North Bridge	-
Controller Hub	Intel® 852GM chipset
FSB	400MHz for 852GM
Display	■ VGA port (1600 x 1200 @ 24bpp 85Hz) ■ 18-bit TTL ■ TV-OUT ■ LVDS (18/36 bit)
Memory	200/266 MHz (No ECC) 200 Pin SODIMM SOCKET(Up to 1GB)

1.3.1.3 Chipset (ICH4)

I/O Interface	LPT	1
	FDD	1
	RS232	3
	RS232/422/485	1 (Default RS232)
	KB	1
	Mouse	1
	IrDA	IrDA1.0 (Optional)

South Bridge	-
Controller Hub	Intel ICH4
PCI Compliant	Supports 33MHz PCI 2.2 specification Supports for 44-bit addressing on PCI using DAC protocol
PCI Bus	■ PCI masters PCI to ISA bridge (W83628F),Support 1 ISA&1 PC104 10/100 LAN(RTL8139DL)
Other Feature	■ 6 USB 2.0 ports, 480 MB/s ■ 2 Ultra ATA (100/66/33 MB/s),Independent timing of up to 4 drives ■ Power Management, ACPI 2.0 compliant ■ FWH interface to Flash BIOS ■ Supports AC'97 2.3 ■ 10/100 Mbit/sec Ethernet support IEEE 802.3 compliant

1.3.1.4 Others(chipset)

LAN	**-**
Chipset	LAN 1: Realtek RTL8139DL for 10/100
IEEE Compliant	Fully compliant with IEEE 802.3
LAN LED	LED0: Off for 10M LAN, Yellow or 100M LAN
	LED1: Green for Link, flash for active,
Disable LAN through BIOS	Yes
Wake on LAN	Yes
Boot from LAN	Yes
LED connector	RJ45 10+4P

Audio	**-**
Chipset	AC97 Audio
Codec	ALC203
Rear panel output	Line-In, Line-out, Mic-In
Amplifier	Yes. (2.2W)

Hardware Monitor	**-**
Chipset	LPC I/O for onboard alarm
	SCH3114
Fan	Programmable automatic fan monitor based on temperature. System FAN Power Connector x 1 It should be added near by the CPU socket Connector type: 2.0mm Wafer box 3x1 Default is +5V Fan Pin1: Fan speed signal input Pin2: +5V Pin3: GND
Temperature	monitors system/CPU temperature and voltage status
Voltage	2.5 V, 1.05 V, 12 V, 5 V, 3.3 V

Super I/O	**-**
Chipset	SCH3114
Fan speed monitor	N/A
Temperature	Yes

1.3.2 Mechanical Specifications

1.3.2.1 Dimension (mm)

203 mm (L) * 146 mm (W) (8" x 5.75")

1.3.2.2 Height on Top (mm)

On board type: 30.5 mm (CPU Heatsink)

Socket type: 30.2 mm (D-SUB COM)

1.3.2.3 Height on Bottom (mm)

5.3 mm (SO-DIMM)

1.3.2.4 Heatsink Dimension (mm)

On board type: 50 x 50 x 30 mm (Heatsink)

Socket type: 51 x 51 x 40 mm (Cooler)

1.3.2.5 Weight(g) with Heatsink

480 g

1.3.3 Electrical Specifications

1.3.3.1 Power Supply Voltage

Power	Power Type	AT / ATX
	Power Supply Voltage	ATX: 5 V Standby, ±5 V ±5%, ±12 V° ±5%, AT: ±5 V ±5%, ±12 V ±5%
	Power Management	APM, ACPI
	Battery	Lithium 3 V

1.3.3.2 Power Supply Current

AT Power:

Test Condition:

OS - WindowsXP SP2

Add-in Card - None

CF Card - Apacer 64M

MiniPCI Card - None

HDD - 40GB IDE *1

BIOS - V1.14

KeyBoard/Mouse - USB or PS/2 Interface

Display - CRT

CPU type	Status	+V5	+V12	+V5	+V12
		512MB*1/533MHz		1GB*1/533MHz	
Intel® Celeron® M 600 MHz	BIOS Picture	2.62A	0.37A	3.02A	0.58A
	DOS Idle	2.51A	0.42A	2.34A	0.23A
	Win Idle	2.24A	0.27A	3.21A	0.67A
	Win HCT11.2	3.22A	0.35A	3.5A	0.49A
	3DMark2001	3.16A	0.43A	4.03A	0.72A

CPU type	Status	+V5	+V12	+V5	+V12
		512MB*1/533MHz		1GB*1/533MHz	
Intel® Celeronl® M 1 GHz	BIOS Picture	1.49A	0.23A	2.93A	0.66A
	DOS Idle	1.25A	0.41A	2.67A	0.61A
	Win Idle	3.33A	0.89A	1.55A	0.44A
	Win HCT11.2	2.91A	0.31A	2.89A	0.36A
	3DMark2001	3.51A	0.18A	3.06A	0.52A

ATX Power:

Test Condition:

OS - WindowsXP SP2
Add-in Card - None
CF Card - Apacer 64M
MiniPCI Card - None
HDD - 40GB IDE *1
BIOS - V1.14
KeyBoard/Mouse - USB or PS/2 Interface
Display - CRT

CPU type	Status	+V5SB	+V5	+V12	+V5SB	+V5	+V12
		512MB*1/533MHz			1GB*1/533MHz		
Intel® Celeron® M 600 MHz	BIOS Picture	0.72A	2.49A	0.53A	0.47A	2.33A	0.41A
	DOS Idle	0.69A	2.23A	0.44A	0.50A	2.06A	0.34A
	S3	0.29A	1.25A	0.24A	0.56A	1.48A	0.42A
	Win Idle	0.33A	1.89A	0.28A	0.74A	2.23A	0.67AA
	Win HCT11.2	0.66A	2.50A	0..53A	0.57A	2.61A	0.41A
	3DMark2001	0.45A	2.43A	0.35A	0.58A	2.82A	0.45

CPU type	Status	+V5SB	+V5	+V12	+V5SB	+V5	+V12
		512MB*1/533MHz			1GB*1/533MHz		
Intel® Celeron® M 1 GHz	BIOS Picture	0.27A	1.34A	0.55A	0.13A	2.52A	0.57A
	DOS Idle	0.26A	1.13A	0.20A	0.24A	2.21A	0.61A
	S3	0.76A	1.66A	0.26A	0.47A	1.68A	0.64A
	Win Idle	0.91A	2.31A	0.35A	0.71A	2.26A	0.21A
	Win HCT11.2	0.59A	2.98A	0.28A	0.43A	2.92A	0.62A
	3DMark2001	0.79A	3.06A	0.64A	0.52A	2.97A	0.76A

1.3.3.3 RTC Battery

Typical Voltage: 3.0 V

Normal discharge capacity: 196 mAh

1.3.4 Environmental Specifications

1.3.4.1 Operating Temperature

The AMD® CPU® is specified for proper operation when the junction temperature is within the specified range of 0° C to 95° C.

The AMD® M690E chipset temperature runs at a maximum of 95° C. The AMD® SB600 I/O Controller case temperature runs at a maximum of 95° C.

Operating temperature: 0 ~ 60° C (32 ~ 140° F)

1.3.4.2 Operating Humidity

0% ~ 90% Relative Humidity, non-condensing

1.3.4.3 Storage Temperature

Standard products (0 ~ 60° C)

Storage temperature: -20 ~ 70° C

1.3.4.4 Storage Relative Humidity

Standard products (0 ~ 60° C)

Relative humidity: 95% @ 60° C

Phoenix products (-20 ~ 80° C)

Relative humidity: 95% @ 60° C

Platinum Phoenix products (-40 ~ 85° C)

Relative humidity: 95% @ 60° C

Chapter 2

H/W Installation

This chapter explains the setup procedures of the POD-6552 hardware, including instructions on setting jumpers and connecting peripherals, switches, indicators and mechanical drawings.

Be sure to read all safety precautions before you begin the installation procedure.

2.1 Jumpers

2.1.1 Jumper List

Label	Function
J1, J2, J3, J4	Setting COM2 RS232/422/485
J5	LCD Voltage Setting
J6	SM BUS Connector
J7	PCI VIO Setting
J8	CMOS Setting
J9	AT / ATX Select

2.1.2 Jumper Settings

J1	**Setting COM2 RS232 / 422 / 485**
Part Number	**1653003201**
Footprint	**JH3X2-2M**
Description	**PIN HEADER 3*2P 180D (M) 2.0 mm DIP SQUARE WO/Pb**
Setting	Function
(1-2)	RS232 (default)
(3-4)	RS422
(5-6)	RS485

J2/J3/J4	**Setting COM2 RS232 / 422 / 485**
Part Number	**1653004101**
Footprint	**JH4X1V-2M**
Description	**PIN HEADER 4*1P 180D (M) 2.0 mm DIP WO/Pb**
Setting	Function
J2(1) ~ J3(1) J2(2) ~ J3(2) J2(3) ~ J3(3) J2(4) ~ J3(4)	RS232
J3(1) ~ J4(1) J3(2) ~ J4(2) J3(3) ~ J4(3) J3(4) ~ J4(4)	RS422 / RS485

J5	**Setting LCD Voltage**
Part Number	**1653003101**
Footprint	**JH3X1V-2M**
Description	**PIN HEADER 3*1P 180D (M) 2.0 mm DIP SQUARE WO/Pb**
Setting	Function
(1-2)	+ 5 V
(2-3)	+ 3.3 V (Default)

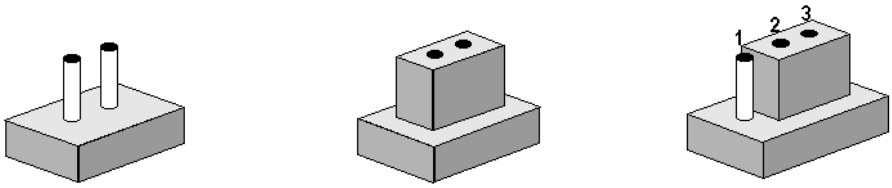
J7	**PCI VIO**
Part Number	**1653003100**
Footprint	**JH3X1V**
Description	**PIN HEADER 3*1P 180D (M) 2.54 mm DIP WO/Pb**
Setting	Function
(1-2)	+ 5 V (default)
(2-3)	+ 3.3 V

J8	**Clear CMOS**
Part Number	**1653002101**
Footprint	**JH2X1V-2M**
Description	**PIN HEADER 2*1P 180D (M) SQUARE 2.0 mm DIP W/O Pb**
Setting	Function
(1-2)	Clear CMOS

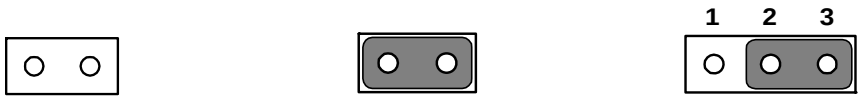
J9	**AT / ATX Select**
Part Number	**1653003101**
Footprint	**JH3X1V-2M**
Description	**PIN HEADER 3*1P 180D (M) 2.0 mm DIP SQUARE WO/Pb**
Setting	Function
(1-2)	ATX Power
(2-3)	AT Power

2.1.3 Jumper Description

Cards can be configured by setting jumpers. A jumper is a metal bridge used to close an electric circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To close a jumper, you connect the pins with the clip. To open a jumper, you remove the clip. Sometimes a jumper will have three pins, labeled 1, 2 and 3. In this case you would connect either pins 1 and 2, or 2 and 3.



The jumper settings are schematically depicted in this manual as follows.



A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes.

Warning! *To avoid damaging the computer, always turn off the power supply before setting jumpers to clear CMOS. Before turning on the power supply, set the jumper back to 3.0 V Battery On.*

2.2 Connectors

2.2.1 Connector List

Label	Function
CN1	VGA D-SUB Connector
CN2	COM Port 1, 2
CN3	TV-OUT Connector
CN4	SUB Port 0,1
CN5	PS/2 Mouse/Keyboard Connector
CN6	LAN Connector
CN7	VGA Connector
CN8	Audio Connector
CN9	COM Port 3, 4
CN10	IrDA Connector
CN11	USB Port 4, 5
CN12	USB Port 2, 3
CN13	PS/2 Connector
CN14	LVDS Connector
CN15	LCD Back Light Connect
CN16	CD-IN Connector
CN17	TTL LCD Connector or DSTN Connector
CN18	PC104 Connector
CN19	ISA Connector
CN20	EBX POWER Connector
CN21	-5 V & -12 V Connector
CN22	CF Connector
CN23	ATX Connector
CN24	Secondary IDE Connector
CN25	Primary IDE Connector
CN26	Panel Connector
CN27	Floppy Connector
CN28	Print Connector
FAN1,2	FAN Connector

2.2.2 Connector Settings

2.2.2.1 COM port connector (CN2, CN9)

COM is the original, yet still common, name of the serial port interface on IBM PC-compatible computers. The POD-6552 provides four serial ports (COM1, COM3, COM4: RS-232 and COM2: RS232/RS422/RS485). CN2 supports COM1 and COM2; CN9 supports COM3, COM4. and J1/J2/J3/J4 is for COM2 RS232/RS422/RS485 selection.

2.2.2.2 USB connectors (CN4, CN11, CN12)

The board provides up to 6* USB (Universal Serial Bus) ports. This gives complete Plug and Play, and hot attach/detach for up to 127 external devices. The USB interfaces comply with USB specification Rev. 2.0 which supports 480Mbps transfer rate, and are fuse protected.

2.2.2.3 VGA connector (CN7)

The DB15-pin female connector is provided for video monitors.

2.2.2.4 Audio Connector (CN8)

The Audio link is a 2x8 pin connector, the POD-6552 can support speaker-out, Line-IN, Line-out with Realtek ALC202, AC97 stereo sound. Detailed pin assignment refer to Appendix A. AC'97 (short for Audio Codec' 97; also MC' 97, short for Modem Codec' 97) is Intel Corporation's Audio "Codec" standard developed by the Intel Architecture Labs in 1997, and used mainly in motherboards, modems, and sound cards.

2.2.2.5 IR connector (CN10)

This connector supports the optional wireless infrared transmitting and receiving module. This module mounts on the system case. You must configure the setting through BIOS setup.

2.2.2.6 PS/2 keyboard and mouse connector (CN13)

PS/2 name comes from the IBM Personal System/2 series of personal computers, with which it was introduced in 1987. The PS/2 mouse connector generally replaced the older DE-9 RS-232 "serial mouse" connector, while the keyboard connector replaced the larger 5-pin DIN used in the IBM PC/AT design.

In most cases, especially in embedded applications, a keyboard is not used. If the keyboard is not present, the standard PC/AT BIOS will report an error or fail during power-on selftest (POST) after a reset. The POD-6552's BIOS standard setup menu allows you to select "All, But Keyboard"under the "Halt On" selection.

This allows no-keyboard operation in embedded system applications, without the system halting under POST.

2.2.2.7 LVDS connector (CN14)

Low-voltage differential signaling, or LVDS, is an electrical signaling system that can run at very high speeds over inexpensive twisted-pair copper cables. LVDS is a differential signaling system, which means that it transmits two different voltages which are compared at the receiver. LVDS uses this difference in voltage between the two wires to encode the information.

POD-6552 uses the Intel 852GM to supports single or dual-channel LVDS panels up to UXGA panel resolution with frequency range from 25 MHz to 112 MHz. Users can connector to 18-bit LVDS LCD with CN14. In addtion, POD-6552 can support 2 channels (2 x 18-bit) LVDS LCD panel (optional).

2.2.2.8 Inverter Connecter (CN15)

POD-6552 can provide +5 V and +12 V and signal to LCD inverter board via CN15.

2.2.2.9 Audio CD-In Connector (CN16)

CD In cable used to send audio CD sound to the computer's audio chipset via CN16.

2.2.2.10 TTL Panel Connector (CN17)

CN17 is a 40-pin connector for TTL LCD or DSTN. It could connect TTL LCD or DSTN freely to meet your need.

2.2.2.11 PC-104 connector (CN18)

POD-6552 supports a PC-104 connector. It is intended for industrial embedded computing environments where applications depend on reliable data acquisition.

2.2.2.12 Power connector (CN20)

POD-6552 can support both ATX and AT power supply and it can use different power cable to do the choice.

1. ATX power supply: you need to use ATX power cable (PN: 1700001112 ATX-20P (M) / 12P (F) 10 CM).
2. AT power supply: you need to use AT power cable (PN: 1700006169 AT Power Cable 6*2P to 10*2P 10 cm).

2.2.2.13 -5 V and -12 V Connector (CN21)

CN20 is secondary power input connector for -5 V and -12 V.

2.2.2.14 CF TYPE I/II Connecter (CN26)

CompactFlash (CF) is a mass storage device format used in portable electronic devices. For storage, CompactFlash typically uses flash memory in a standardized enclosure.

POD-6552 has s CF slot and it can support CompactFlash card type I/II and it occupies a secondary IDE channel which can be enabled/disabled via the BIOS settings.

2.2.2.15 IDE Connector (CN24_CN25)

The POD-6552 provides two IDE channels so you can attach up to four Enhanced Integrated Device Electronics hard disk drives or CDROM to the POD-6552's internal controller. The POD-6552's IDE controller uses a PCI interface. This advanced IDE controller supports faster data transfer, PIO Mode 3 or Mode 4, UDMA 100 mode.

How to connect the hard drive to CN24 or CN25

Connecting drives is done in a daisy-chain fashion. It requires one of two cables (not included in this package), depending on the drive size. 1.8" and 2.5" drives need a 1 x 44-pin to 2 x 44-pin flat-cable connector. 3.5" drives use a 1 x 44-pin to 2 x 40-pin connector. Wire number 1 on the cable is red or blue, and the other wires are gray.

1. Connect one end of the cable to CN16. Make sure that the red (or blue) wire corresponds to pin 1 on the connector, which is labeled on the board (on the right side).
2. Plug the other end of the cable into the Enhanced IDE hard drive, with pin 1 on the cable corresponding to pin 1 on the hard drive.

2.2.2.16 Front Panel Connecter (CN26)

CN26 is a 2x7 pin header for front panel. It support reset, power & hard disk indicator. The function is defined as follow.

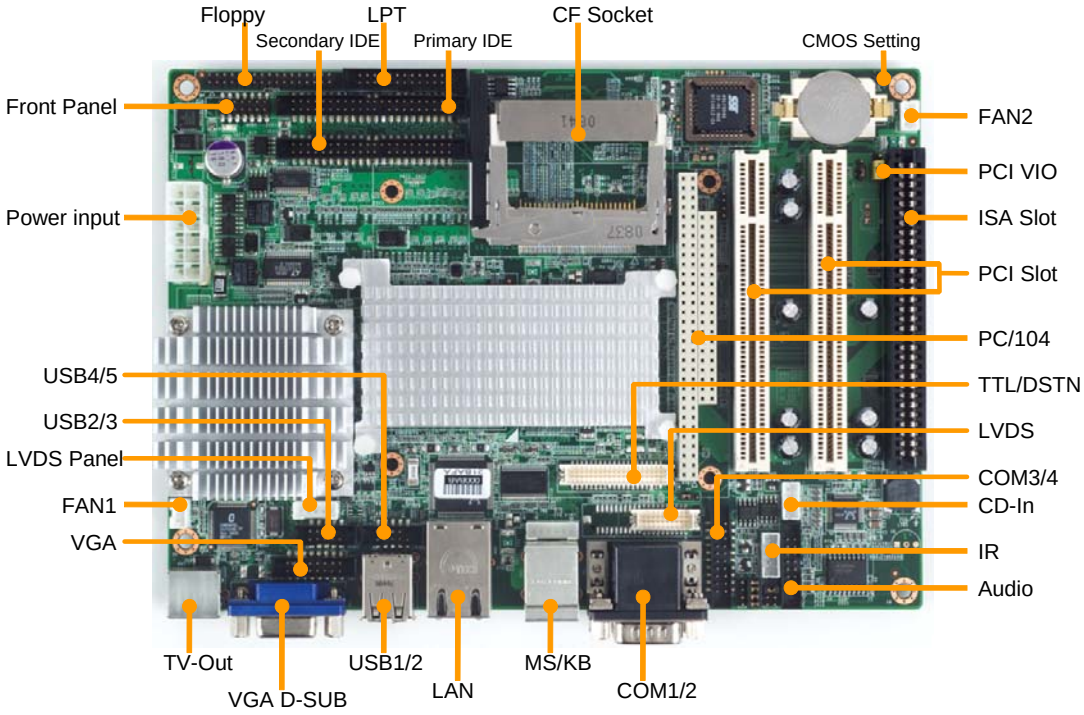
- HDD LED (Pin 1 & Pin2)
- Power LED (Pin 3 & Pin 4)
- Suspend LED (Pin 5 & Pin 6)
- Lan Active LED (Pin 7 & Pin 8)
- Lan Linked LED (Pin 9 & Pin10)
- Power Button (Pin 11 & Pin12)
- Reset (Pin 13 & Pin14)

2.2.2.17 LPT Connector (CN28)

POD-6552 support a multi-mode (ECP/EPP/SPP) parallel port accessed via CN28 and a 26-pin flat-cable. The parallel port is designated as LPT1, and can be disabled or changed to LPT2 or LPT3 in the system BIOS setup. The parallel port interrupt channel is designated to be IRQ7. You can select ECP/EPP DMA channel via BIOS setup.

2.3 Mechanical

2.3.1 Jumper and Connector Location



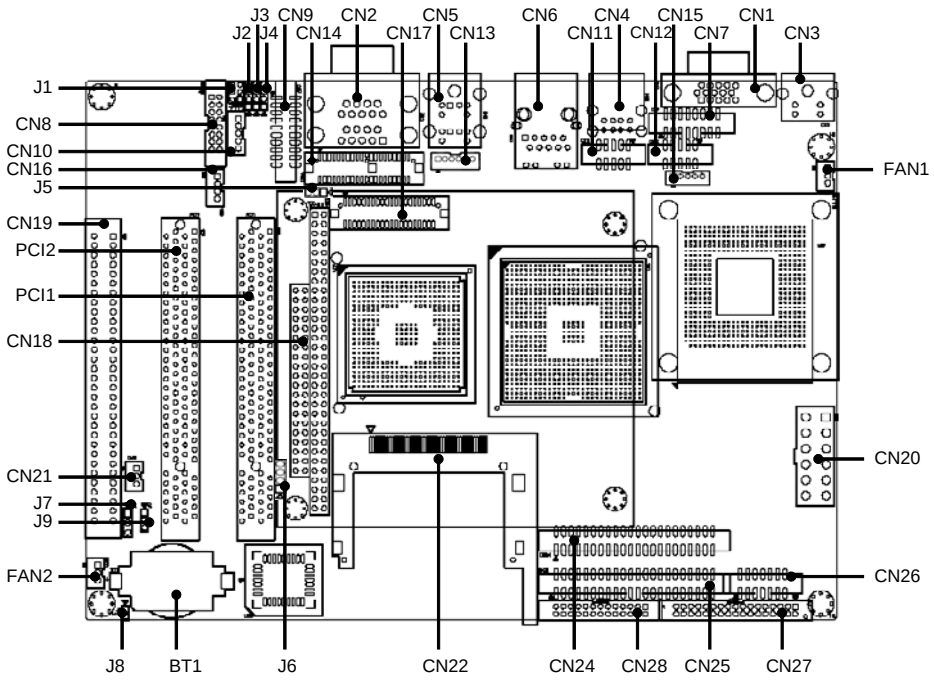


Figure 2.1 Jumper and Connector Layout (Component Side)

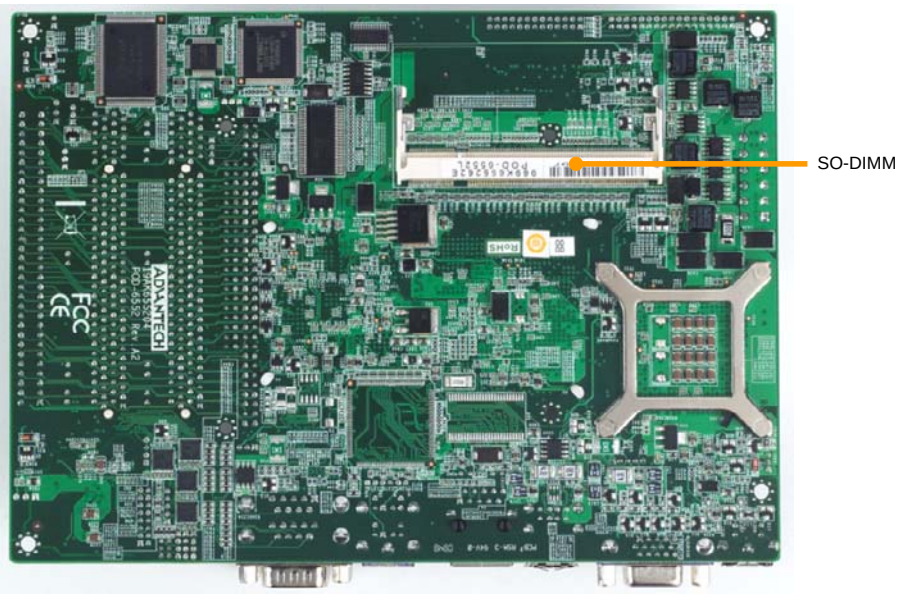


Figure 2.2 Jumper and Connector Layout (Solder Side)

2.3.2 Board Dimension

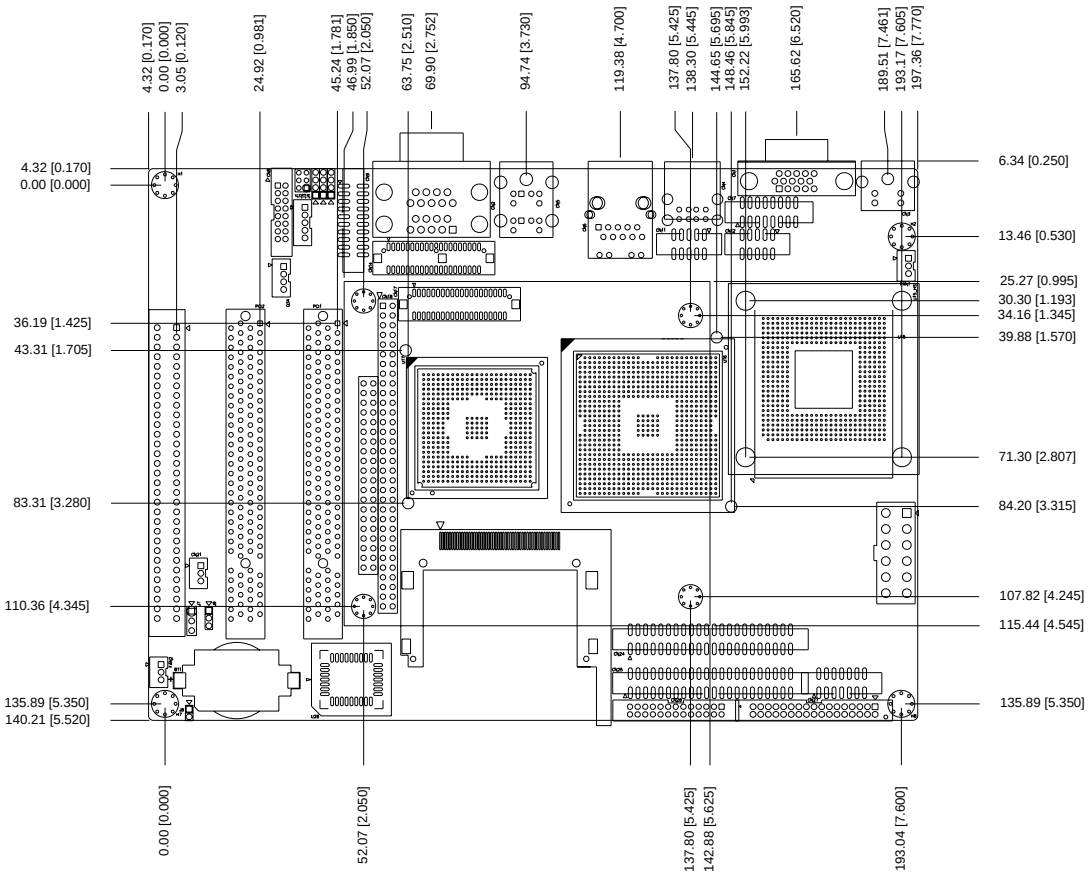


Figure 2.3 Board Dimension Layout (Component Side)

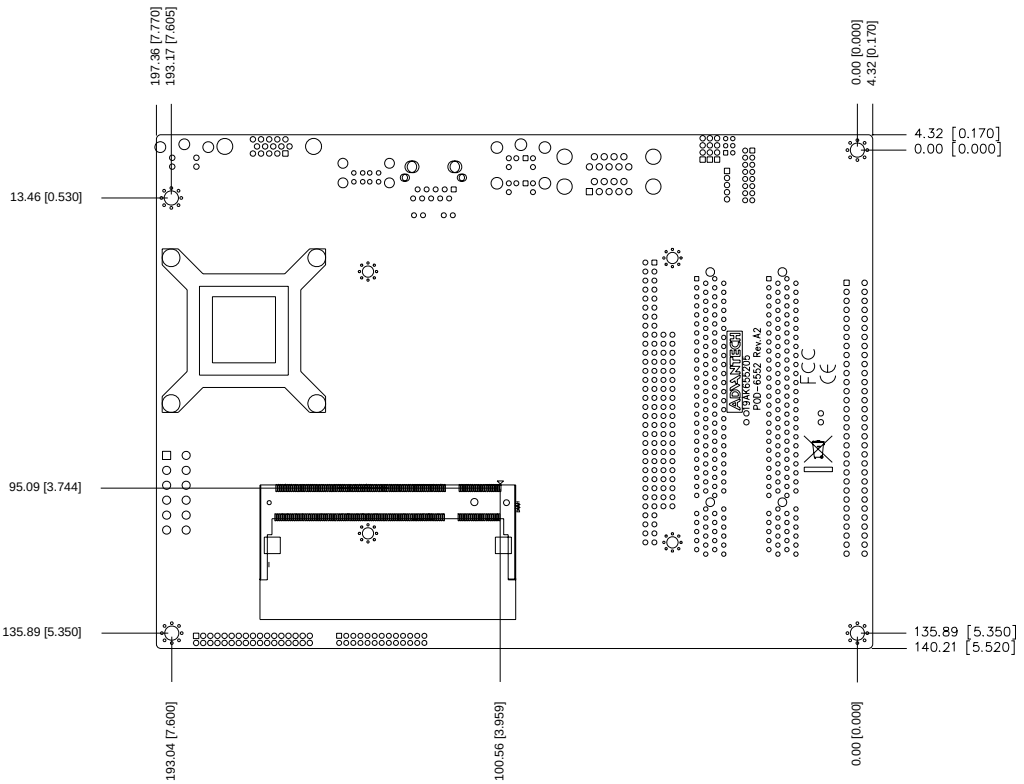


Figure 2.4 Board Dimension Layout (Solder Side)

Chapter 3

BIOS Operation

Sections include:

- **BIOS Introduction**
- **BIOS Setup**

3.1 BIOS Introduction

AwardBIOS 6.0 is a full-featured BIOS provided by Advantech to deliver superior performance, compatibility, and functionality to industrial PCs and embedded boards. Its many options and extensions let you customize your products to a wide range of designs and target markets.

The modular, adaptable AwardBIOS 6.0 supports the broadest range of third-party peripherals and all popular chipsets, plus Intel, AMD, nVidia, VIA, and compatible CPUs from 386 through Pentium, AMD Geode, K7 and K8 (including multiple processor platforms), and VIA Eden C3 and C7 CPUs.

You can use Advantech's utilities to select and install features that suit your needs and your customers' needs.

3.2 BIOS Setup

The POD-6552 system has AwardBIOS 6.0 built-in, which includes a CMOS SETUP utility that allows users to configure settings as required or to activate certain system features.

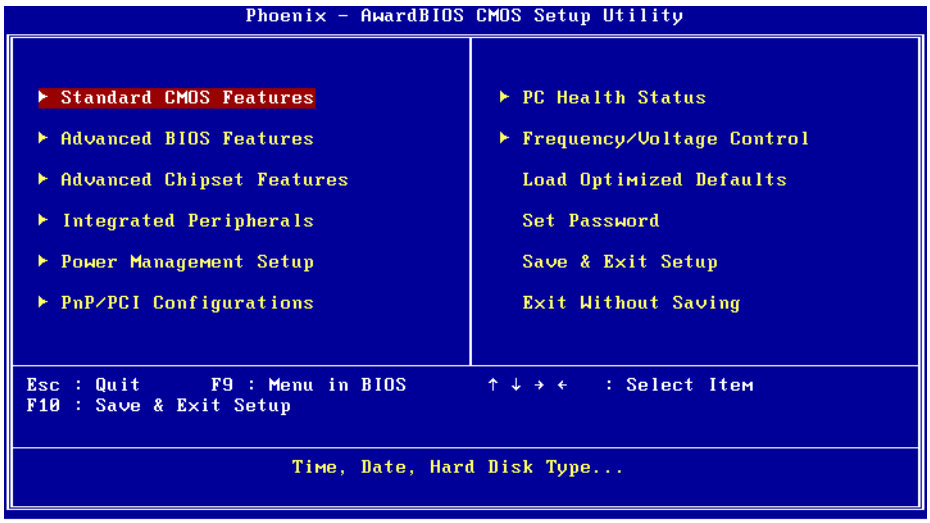
The CMOS SETUP saves configuration settings in the CMOS RAM of the motherboard. When the system power is turned off, the onboard battery supplies the necessary power to the CMOS RAM so that settings are retained.

To access the CMOS SETUP screen, press the <Del> button during the power-on BIOS POST (Power-On Self Test).

CMOS SETUP Navigation and Control Keys	
< ↑ >< ↓ >< ← >< → >	Move to highlight item
<Enter>	Select Item
<Esc>	Main Menu - Start Quit sequence
	Sub Menu - Exit the current page and return to level above
<Page Up/+>	Increase the numeric value or make changes
<Page Down/->	Decrease the numeric value or make changes
<F1>	General help, for Setup Sub Menu
<F2>	Item Help
<F5>	Load Previous Values
<F7>	Load Optimized Defaults
<F10>	Save all CMOS changes

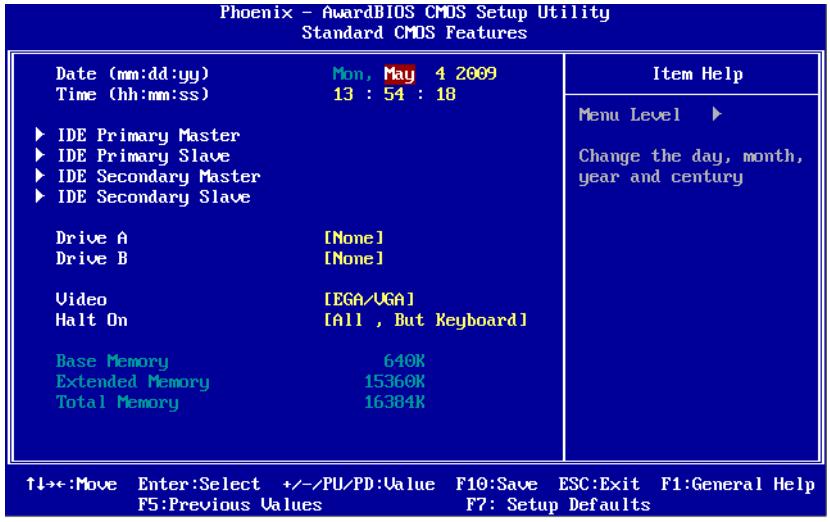
3.2.1 Main Menu

Press the <Del> key during startup to enter the BIOS CMOS Setup Utility; the Main Menu will appear on the screen. Use arrow keys to highlight the desired item, and press <Enter> to accept, or enter the sub-menu.



- **Standard CMOS Features**
  This setup page includes all the features for standard CMOS configuration.
- **Advanced BIOS Features**
  This setup page includes all the features for advanced BIOS configuration.
- **Advanced Chipset Features**
  This setup page includes all the features for advanced chipset configuration.
- **Integrated Peripherals**
  This setup page includes all onboard peripheral devices.
- **Power Management Setup**
  This setup page includes all the power management items.
- **PnP/PCI Configurations**
  This setup page includes PnP OS and PCI device configuration.
- **PC Health Status**
  This setup page includes the system auto-detect CPU and system temperature, voltage, and fan speed.
- **Frequency/Voltage Control**
  This setup page includes CPU host clock control, frequency ratio and voltage.
- **Load Optimized Defaults**
  This selection loads optimized values for best system performance configuration.
- **Set Password**
  Establish, change or disable passwords.
- **Save & Exit Setup**
  Save CMOS value settings to CMOS and exit BIOS setup.
- **Exit Without Saving**
  Abandon all CMOS value changes and exit BIOS setup.

3.2.2 Standard CMOS Features


Phoenix - AwardBIOS CMOS Setup Utility
Standard CMOS Features
Date (mm:dd:yy) Mon, May 4 2009
Time (hh:mm:ss) 13 : 54 : 18
IDE Primary Master
IDE Primary Slave
IDE Secondary Master
IDE Secondary Slave
Drive A [None]
Drive B [None]
Video [EGA/VGA]
Halt On [All , But Keyboard]
Base Memory 640K
Extended Memory 15360K
Total Memory 16384K
Item Help
Menu Level
Change the day, month, year and century
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help
F5:Previous Values F7: Setup Defaults

- **Date**

  The date format is <weekday>, <month>, <day>, <year>.

Weekday	From Sun to Sat, determined and displayed by BIOS only
Month	From Jan to Dec.
Day	From 1 to 31
Year	From 1999 through 2098

- **Time**

  The time format is <hours> : <minutes> : <seconds>, based on 24-hour time.

- **IDE Primary/Secondary Master/Slave**

  IDE HDD Auto-Detection - Press "Enter" for automatic device detection.

- **Drive A / Drive B**

  The Item identifies the types of floppy disk drive A or drive B

None	No floppy drive installed
360K, 5.25"	5.25 inch PC-type standard drive; 360K byte capacity
1.2M, 5.25"	5.25 inch AT-type high-density drive; 1.2M byte capacity
720K, 3.5"	3.5 inch double-sided drive; 720K byte capacity
1.44M, 3.5"	3.5 inch double-sided drive; 1.44M byte capacity
2.88M, 3.5"	3.5 inch double-sided drive; 2.88M byte capacity

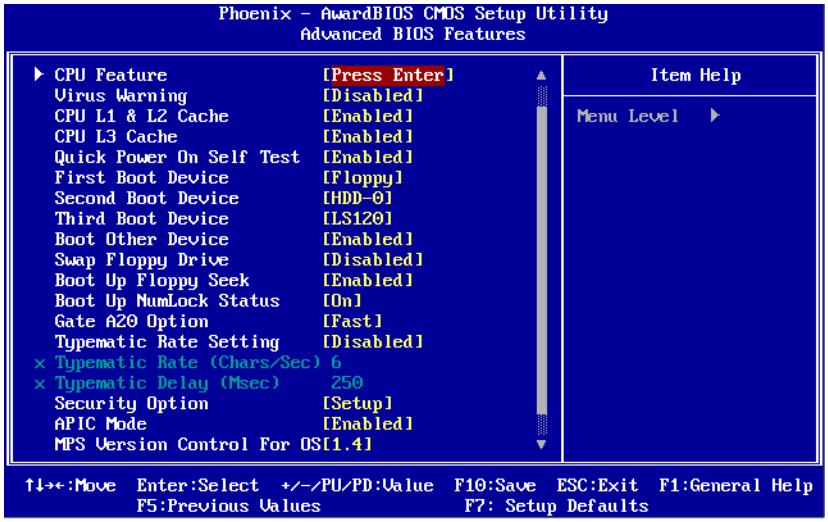
- **Halt on**

  This item determines whether the computer will stop if an error is detected during power up.

No Errors	The system boot process will not stop for any error
All Errors	Whenever the BIOS detects a non-fatal error the system boot process will be stopped.
All, But Keyboard	The system boot process will not stop for a keyboard error, but will stop for all other errors. (Default value)
All, But Diskette	The system boot process will not stop for a diskette error, but will stop for all other errors.
All, But Disk/Key	The system boot process will not stop for a keyboard or disk error, but will stop for all other errors.

- **Base Memory**
  Displays the amount of base (or conventional) memory installed in the system.
- **Extended Memory**
  Displays the amount of extended memory (above 1 MB in CPU°Øs memory address map) installed in the system.
- **Total Memory**
  Displays the total system memory size.

3.2.3 Advanced BIOS Features


Phoenix - AwardBIOS CMOS Setup Utility
Advanced BIOS Features
CPU Feature [Press Enter]
Virus Warning [Disabled]
CPU L1 & L2 Cache [Enabled]
CPU L3 Cache [Enabled]
Quick Power On Self Test [Enabled]
First Boot Device [Floppy]
Second Boot Device [HDD-0]
Third Boot Device [LS120]
Boot Other Device [Enabled]
Swap Floppy Drive [Disabled]
Boot Up Floppy Seek [Enabled]
Boot Up NumLock Status [On]
Gate A20 Option [Fast]
Typematic Rate Setting [Disabled]
x Typematic Rate (Chars/Sec) 6
x Typematic Delay (Msec) 250
Security Option [Setup]
APIC Mode [Enabled]
MPS Version Control For OS[1.4]
Item Help
Menu Level
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help
F5:Previous Values F7: Setup Defaults

- **CPU Feature**
  This item allows the user to adjust CPU settings such as CPU ratio, VID and Thermal, and special features like XD flag.
- **CPU L1 & L2 Cache [Enabled]**
  This item allows user to enable CPU L1 & L2 cache.
- **CPU L3 Cache [Enabled]**
  This item allows the user to enable/disable CPU L3 cache.
- **Quick Power On Self Test [Enabled]**
  This field speeds up the Power-On Self Test (POST) routine by skipping re-testing a second, third and fourth time. The default setting is enabled.
- **First / Second / Third / Other Boot Drive**

Floppy	Select boot device priority by Floppy
Hard Disk	Sets boot priority for the hard disk.
CDROM	Sets boot priority for CDROM.
USB-FDD	Sets boot priority for USB-FDD.
USB-ZIP	Sets boot priority for USB-ZIP.
USB-CDROM	Sets boot priority for USB-CDROM.
LAN	Sets boot priority for LAN.
Disabled	Disables this boot function.

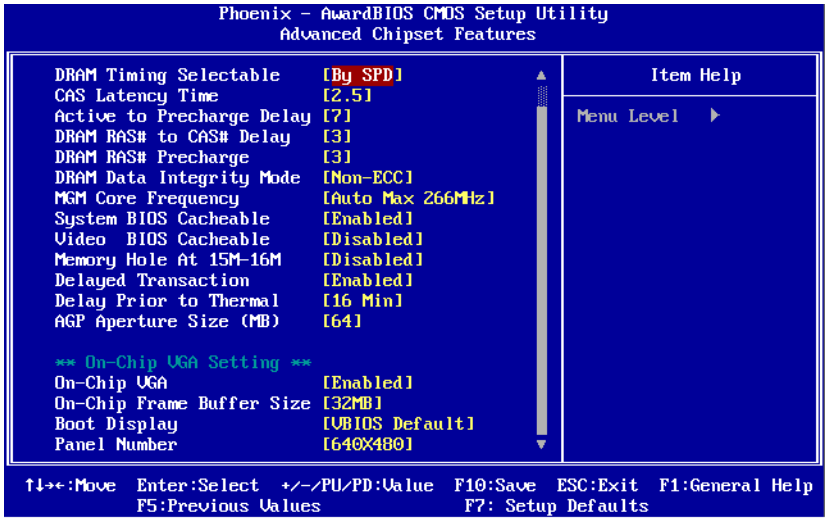
- **Swap Floppy Drive [Disabled]**
  This item enables users to swap floppy “A” and “B” identified without change hardware cable connection.

- **Boot Up Floppy Seek [Disabled]**
  When enabled, the BIOS will seek the floppy “A” drive one time.
- **Boot Up NumLock Status [Enabled]**
  This item allows the user to activate the Number Lock key at system boot.
- **Gate A20 Option [Fast]**
  This item allows the user to switch on or off A20 control by port 92.
- **Typematic Rate Setting**
  This item allows the user to set the two typematic control items.
  This field controls the speed of
  – Typematic Rate (Chars/Sec)
    This item controls the speed at which the system registers auto repeated keystrokes.
    The eight settings are: 6, 8, 10, 12, 15, 20, 24 and 30.
  – Typematic Delay (Msec)
    This item sets the key press delay time before auto repeat begins. The four delay rate options are: 250, 500, 750 and 1000.
- **Security Option [Setup]**

System	System requires correct password before booting, and also before permitting access to the Setup page.
Setup	System will boot, but requires correct password before permitting access to Setup. (Default value)

- **APIC Mode [Enabled]**
  This item allows the user to enable/disable the Advanced Programmable Interrupt Controller. APIC is implemented in the motherboard and must be supported by the operating system; it extends the number of IRQs available.
- **MPS Version Control for OS [1.4]**
  This item sets the operating system multiprocessor support version.
- **OS Select For DRAM > 64 MB [Non-OS2]**
  Select OS2 only if the system is running the OS/2 operating system with greater than 64 MB of RAM on the system.

3.2.4 Advanced Chipset Features


Phoenix - AwardBIOS CMOS Setup Utility
Advanced Chipset Features
DRAM Timing Selectable [By SPD]
CAS Latency Time [2.5]
Active to Precharge Delay [7]
DRAM RAS# to CAS# Delay [3]
DRAM RAS# Precharge [3]
DRAM Data Integrity Mode [Non-ECC]
MGM Core Frequency [Auto Max 266Mhz]
System BIOS Cacheable [Enabled]
Video BIOS Cacheable [Disabled]
Memory Hole At 15M-16M [Disabled]
Delayed Transaction [Enabled]
Delay Prior to Thermal [16 Min]
AGP Aperture Size (MB) [64]
** On-Chip VGA Setting **
On-Chip VGA [Enabled]
On-Chip Frame Buffer Size [32MB]
Boot Display [VBIOS Default]
Panel Number [640X480]
Item Help
Menu Level
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help
F5:Previous Values F7: Setup Defaults

Note! *The "Advanced Chipset Features" screen controls the configuration of the board's chipset register settings and performance tuning - the options on this screen may vary depending on the chipset type. It is strongly recommended that only technical users make changes to the default settings.*

- **DRAM Timing Selectable [By SPD]**

  This item allows the user to set optimal timings for items 2 through 5. The system default setting of “By SPD” follows the SPD information on the ROM chip and ensures the system runs stably, with optimal performance.

- **CAS Latency Time [2.5]**

  This item allows the user to set the timing delay in clock cycles before SDRAM starts a read command after receiving it.

- **DRAM RAS# to CAS# Delay [3]**

  This item allows the user to set the timing of the transition from RAS (row address strobe) to CAS (column address strobe) as both rows and columns are separately addressed shortly after the DRAM is refreshed.

- **DRAM RAS# Precharge [3]**

  This item allows the user to set the DRAM RAS# precharge timing. The system default is set to “Auto” to reference the data from the SPD ROM.

- **Active to Precharge Delay [7]**

  This item allows the user to adjust memory precharge time.

- **MGM Core Frequency [Auto Max 266 Mhz]**

  This item enables users to set the operation speed of internal Graphic Chip FSB and DRAM , system default is setting to “Auto Max 266 MHz” to reference value..

- **System BIOS Cacheable [Enabled]**

  This item allows the system BIOS to be cached to allow faster execution and better performance.

- **Video BIOS Cacheable [Disabled]**

  This item allows the video BIOS to be cached to allow faster execution and better performance.

- **Memory Hole At 15 M-16 M [Disabled]**

  This item reserves 15 - 16 MB of memory address space for ISA expansion cards that specifically require the setting. Memory from 15 - 16 MB will be unavailable to the system because only the expansion cards can access memory in this area.

- **Delayed Transaction [Enabled]**

  This items enables users to actives PCI delayed Transaction feature, it can have better PCI performance and meet PCI 2.1 specifications.

- **Delay Period to Thermal [16 Min]**

  This items enables users to select the time period of system detect CPU Thermal, system default is setting to “16 Min” to reference value.

- **AGP Aperture Size (MB) [64]**

  This item enables users to select size of system memory to support AGP graphic usage, system default is setting to “64 MB” to reference value.

- **On-Chip VGA [Enabled]**

  This item enables users to Enabled or Disabled On-Chip VGA device, system default is setting to “Enabled” to reference value.

- **On-Chip Frame Buffer Size [32 MB]**

  This item allows the user to adjust the memory buffer for on-chip graphics.

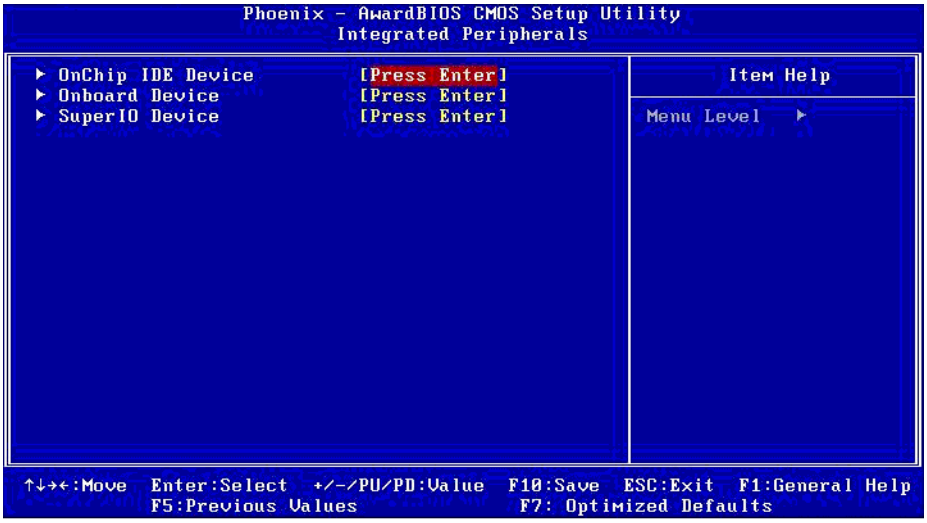
- **Boot Display [VBIOS Default]**

  This item allows the user to decide which display mode to use for the boot display.

- **Panel Type [640 x 480]**

  This item allows the user to adjust panel resolution.

3.2.5 Integrated Peripherals


Phoenix - AwardBIOS CMOS Setup Utility
Integrated Peripherals
OnChip IDE Device [Press Enter]
Onboard Device [Press Enter]
SuperIO Device [Press Enter]
Item Help
Menu Level
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help
F5:Previous Values F7: Optimized Defaults

Note! *The "Integrated Peripherals" screen controls chipset configuration for IDE, ATA, SATA, USB, AC97, MC97 and Super IO and Sensor devices. The options on this screen vary depending on the chipset.*

- **OnChip IDE Device**

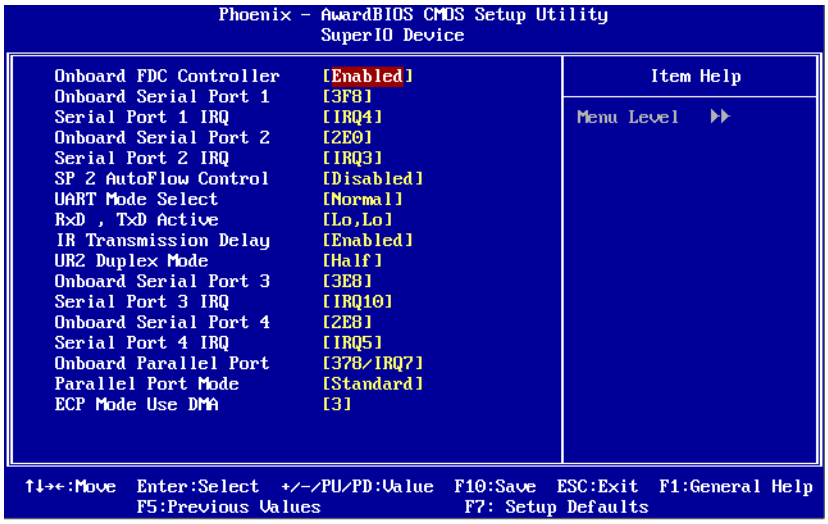
  This item enables users to set the OnChip IDE device status, including IDE devices and setting PIO and DMA access modes. Some chipsets support newer SATA devices (Serial-ATA).

- **Onboard Device**

  This item enables users to set the Onboard Device status, including USB, AC97, MC97 and LAN devices.

- **Super IO Device**

  This item enables users to set the Super IO device status, including Floppy, COM, LPT, IR and to control GPIO and Power fail status.

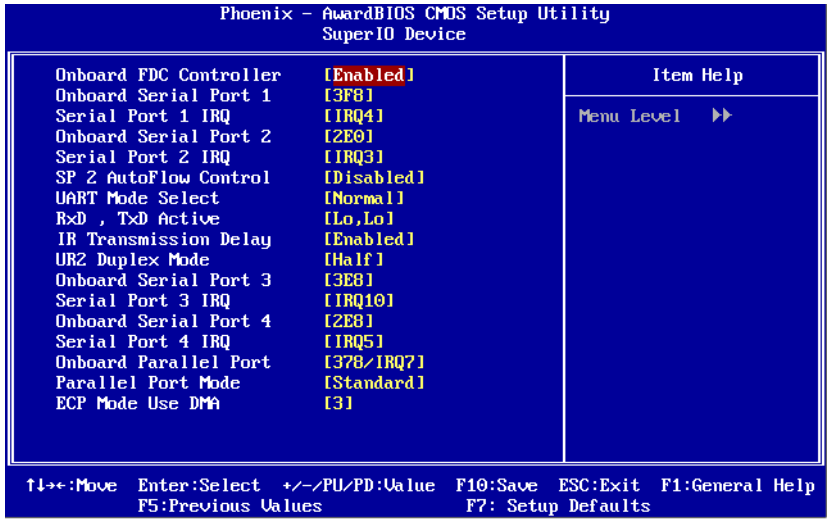

Phoenix - AwardBIOS CMOS Setup Utility
SuperIO Device
Onboard FDC Controller [Enabled]
Onboard Serial Port 1 [3F8]
Serial Port 1 IRQ [IRQ4]
Onboard Serial Port 2 [2E0]
Serial Port 2 IRQ [IRQ3]
SP 2 AutoFlow Control [Disabled]
UART Mode Select [Normal]
RxD , TxD Active [Lo,Lo]
IR Transmission Delay [Enabled]
UR2 Duplex Mode [Half]
Onboard Serial Port 3 [3E8]
Serial Port 3 IRQ [IRQ10]
Onboard Serial Port 4 [2E8]
Serial Port 4 IRQ [IRQ5]
Onboard Parallel Port [378/IRQ7]
Parallel Port Mode [Standard]
ECP Mode Use DMA [3]
Item Help
Menu Level
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help
F5:Previous Values F7: Setup Defaults

- **Onboard Serial port 1 [3F8]**

  This item allows the user to adjust serial port 1 address.

- **Serial port 1 IRQ [IRQ4]**
  This item allows the user to adjust serial port 1 IRQ.
- **Onboard Serial port 2 [2F8]**
  This item allows the user to adjust serial port 2 address.
- **Serial port 2 IRQ [IRQ3]**
  This item allows the user to adjust serial port 2 IRQ.
- **Onboard Serial port 3 [3E8]**
  This item allows the user to adjust serial port 3 address.
- **Serial port 3 IRQ [IRQ10]**
  This item allows the user to adjust serial port 3 IRQ.
- **Onboard Serial port 4 [2E8]**
  This item allows the user to adjust serial port 4 address.
- **Serial port 4 IRQ [IRQ5]**
  This item allows the user to adjust serial port 4 IRQ.
- **Onboard Parallel Port [378/IRQ7]**
  This item allows the user to adjust parallel port address and IRQ.
- **Parallel Port Mode [Standard]**
  This item allows the user to adjust parallel port mode.
- **ECP Mode Use DMA [3]**
  This item allows the user to adjust the ECP DMA resource.

3.2.6 Power Management Setup


Phoenix - AwardBIOS CMOS Setup Utility
SuperIO Device
Onboard FDC Controller [Enabled]
Onboard Serial Port 1 [3F8]
Serial Port 1 IRQ [IRQ4]
Onboard Serial Port 2 [2E0]
Serial Port 2 IRQ [IRQ3]
SP 2 AutoFlow Control [Disabled]
UART Mode Select [Normal]
RxD , TxD Active [Lo,Lo]
IR Transmission Delay [Enabled]
UR2 Duplex Mode [Half]
Onboard Serial Port 3 [3E8]
Serial Port 3 IRQ [IRQ10]
Onboard Serial Port 4 [2E8]
Serial Port 4 IRQ [IRQ5]
Onboard Parallel Port [378/IRQ7]
Parallel Port Mode [Standard]
ECP Mode Use DMA [3]
Item Help
Menu Level
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help
F5:Previous Values F7: Setup Defaults

Note! *The "Power Management Setup" screen allows configuration of the system for effective energy savings while still operating in a manner consistent with intended computer use.*

- **ACPI Function [Enabled]**
  This item defines the ACPI (Advanced Configuration and Power Management) feature that makes hardware status information available to the operating system, and communicates to PC and system devices for improved power management.

- **ACPI Suspend Type [S1 (POS)]**

  This item allows the user to select the sleep state when the computer is in suspend mode.

S1(POS)	Suspend mode is equivalent to a software power down;
S3(STR)	The system shuts down with the exception of a refresh of electrical current to system memory.

- **Power Management [Min Saving]**

  This item allows the user to select the system power saving mode.

  – Min Saving - Minimum power management. Suspend Mode=1 hr.
  – Max Saving - Maximum power management. Suspend Mode=1 min.
  – User Defined - Allows the user to set each mode individually. Suspend Mode= Disabled, or 1 min ~ 1 hr.

- **Video Off Method [DPMS]**

  This item allows the user to determine the manner is which the monitor is blanked.

V/H SYNC+Blank	This option will cause the system to turn off vertical and horizontal synchronization ports and write blanks to the video buffer.
Blank Screen	This option only writes blanks to the video buffer.
DPMS	Initial display power management signaling.

- **Video Off In Suspend [Yes]**

  This item allows the user to turn off the video when the system enters suspend mode.

- **Suspend Type [Stop Grant]**

  This item allows the user to determine the suspend type.

- *Modem Use IRQ [3]*

  This item allows the user to determine which IRQ the MODEM can use.

- **Suspend Mode [1 Hour]**

  This item allows the user to determine the length of time of system inactivity after which all devices except the CPU will be shut down.

- **HDD Power Down Mode [15 Min]**

  This item allows the user to determine the system inactivity time, when the hard disk drive will be powered down.

- **Soft-Off by PWR-BTTN [Instant-Off]**

  This item allows the user to define the power button functions.

Instant-Off	Press the power button to power off instantly.
Delay 4 Sec	Press and hold the power button for 4 sec to power off.

- **PWRON After PWR-Fail [Former-Sts]**

  This item allows the user to select recovery after power fail function; this function depends on the chipset.

- **Power On by LAN [Enabled]**

  This item allows the user to enable and define how LAN wake the system up from suspend mode.

- **Power On by Ring [Enabled]**

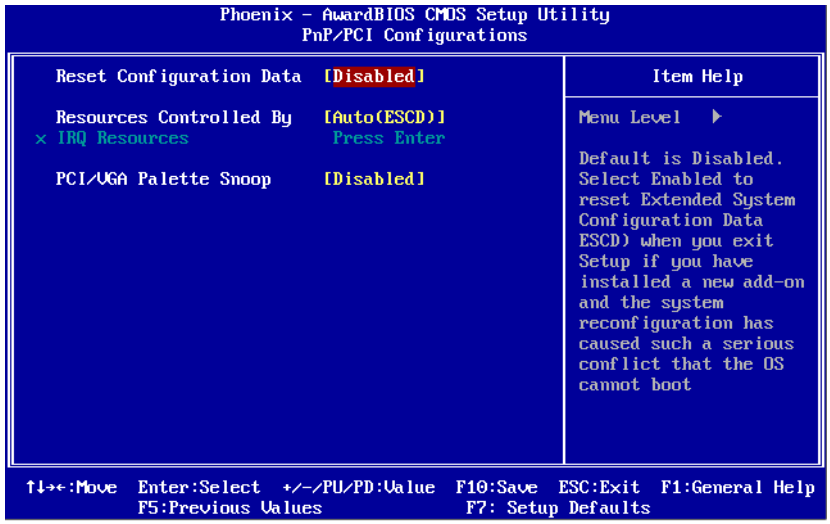
  This item allows the user to enable and define how the system will resume by activation of the modem ring.

- **Resume by Alarm [Disabled]**

  This item allows the user to enable and key in the date and time to power on the system

Disabled	Disable this function.
Enabled	Enable alarm function to power on system
Day (of month)	Alarm 1-31
Time (HH:MM:SS)	Alarm (0-23) : (0-59) : 0-59)

3.2.7 PnP/PCI Configurations


Phoenix - AwardBIOS CMOS Setup Utility
PnP/PCI Configurations
Reset Configuration Data [Disabled]
Resources Controlled By [Auto(ESCD)]
× IRQ Resources Press Enter
PCI/VGA Palette Snoop [Disabled]
Item Help
Menu Level ▶
Default is Disabled. Select Enabled to reset Extended System Configuration Data ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the OS cannot boot
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help
F5:Previous Values F7: Setup Defaults

Note! *The "PnP/PCI Configurations" screen sets up the IRQ and DMA (both PnP and PCI bus assignments).*

- **Reset Configuration Data [Disabled]**

  This item allows the user to clear any PnP configuration data stored in the BIOS.

- **Resources Controlled By [Auto (ESCD)]**
  - IRQ Resources

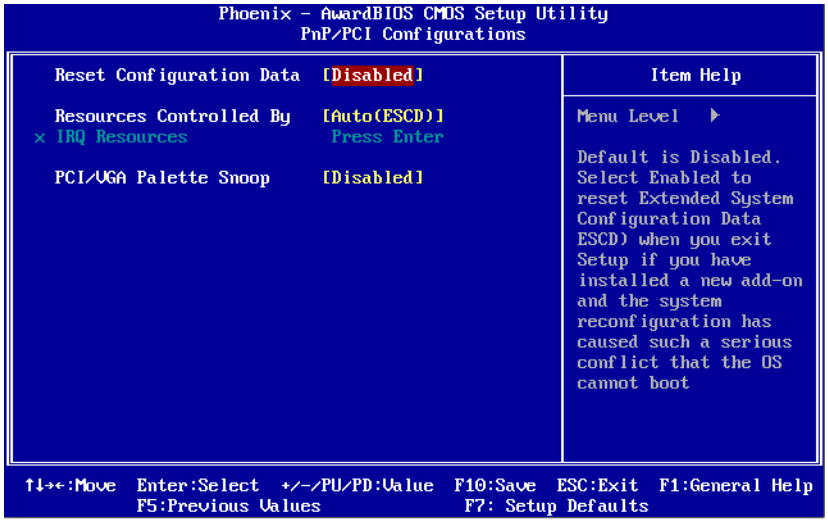
    This item allows you respectively assign an interrupt type for IRQ-3, 4, 5, 7, 9, 10, 11, 12, 14, and 15.
  - DMA Resources

    This item allows you respectively assign an interrupt type for DMA-0, 1, 2, 3, 4, 5, 6, and 7.

- **PCI VGA Palette Snoop [Disabled]**

  The item is designed to solve problems caused by some non-standard VGA cards. A built-in VGA system does not need this function.

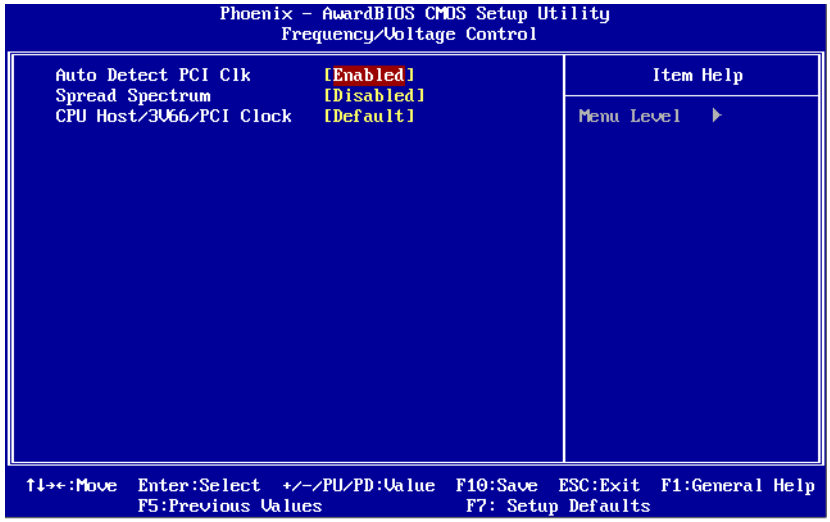
3.2.8 PC Health Status


Phoenix - AwardBIOS CMOS Setup Utility
PnP/PCI Configurations
Reset Configuration Data [Disabled]
Resources Controlled By [Auto(ESCD)]
× IRQ Resources Press Enter
PCI/VGA Palette Snoop [Disabled]
Item Help
Menu Level ▶
Default is Disabled. Select Enabled to reset Extended System Configuration Data ESCD) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the OS cannot boot
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help
F5:Previous Values F7: Setup Defaults

Note! *The "PC Health Status" screen controls the thermal, fan, and voltage status of the board. The options on this page vary depending on the chipset.*

- **Shutdown Temperature [60° C/140° F]**
  This item enables users to set the limitation of CPU temperature, the range is from 85° C through 100° C.
- **Current CPU /System Temperature [Show Only]**
  This item displays current CPU/System temperature.
- **FAN 1 / FAN2 Speed [Show Only]**
  This item displays current system FAN(s) speed(s).
- **3.3 V/ 1.05 V/2.5 V/ 5 V/ 12 V [Show Only]**
  This item displays current CPU and system voltage.

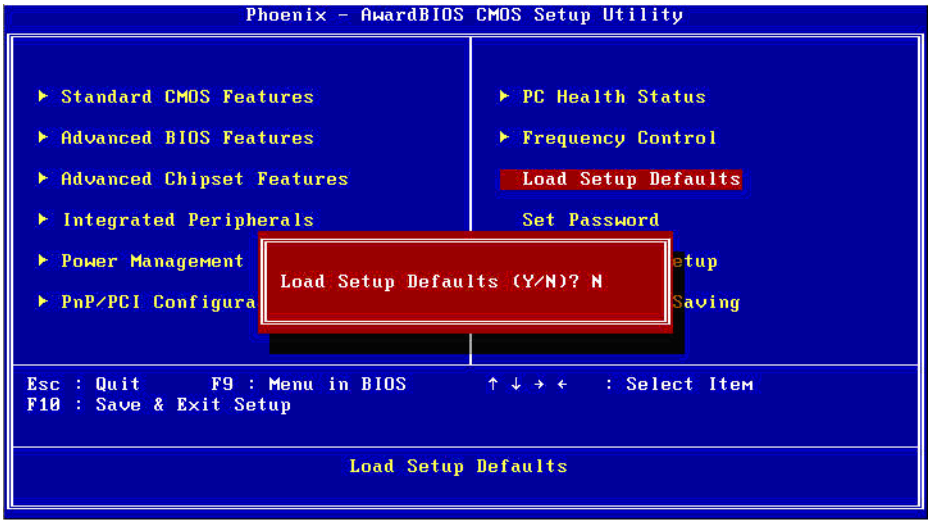
3.2.9 Frequency/Voltage Control


Phoenix - AwardBIOS CMOS Setup Utility
Frequency/Voltage Control
Auto Detect PCI Clk [Enabled]
Spread Spectrum [Disabled]
CPU Host/3V66/PCI Clock [Default]
Item Help
Menu Level
↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help
F5:Previous Values F7: Setup Defaults

Note! *The "Frequency/Voltage Control" screen controls the CPU host and PCI frequency. The options on this page vary depending on the chipset; items show up according to installed CPU capacities.*

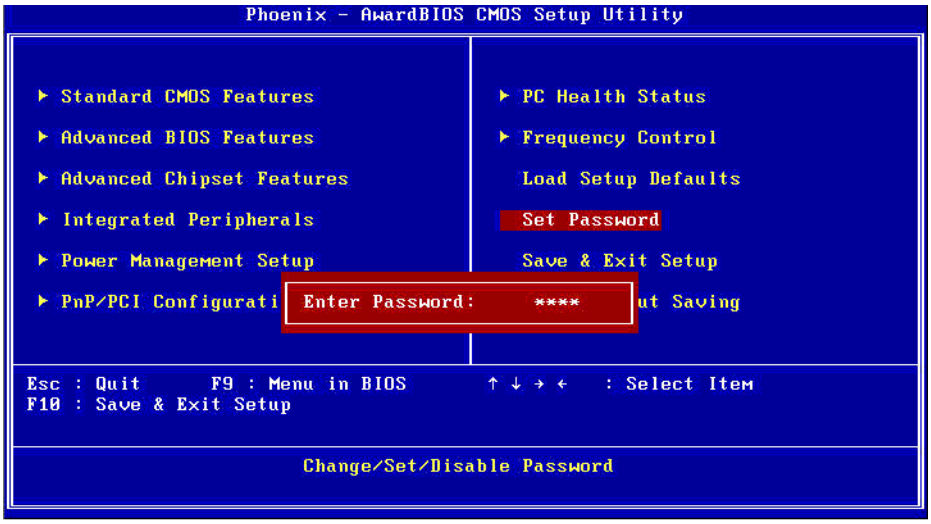
- **Auto Detect PCI Clk [Enabled]**
  This item enables users to set the PCI Clk either by automatic system detection or manually.
- **Spread Spectrum [Disabled]**
  This item enables users to set the spread spectrum modulation.
- **CPU Host/SRC/PCI Clock [Default]**
  This item enables users to set the CPU Host and PCI clock by system automatic detection or by manual

3.2.10 Load Optimized Defaults


Phoenix - AwardBIOS CMOS Setup Utility
Standard CMOS Features
Advanced BIOS Features
Advanced Chipset Features
Integrated Peripherals
Power Management
PnP/PCI Configura
PC Health Status
Frequency Control
Load Setup Defaults
Set Password
Load Setup Defaults (Y/N)? N
Esc : Quit F9 : Menu in BIOS ↑ ↓ → ← : Select Item
F10 : Save & Exit Setup
Load Setup Defaults

Note! *"Load Optimized Defaults" loads the default system values directly from ROM. If the stored record created by the setup program should ever become corrupted (and therefore unusable), select Load Setup Defaults to have these default values load automatically for the next bootup.*

3.2.11 Set Password



Note! *To enable this feature, you should first go to the "Advanced BIOS Features" menu, choose the Security Option, and select either System or Setup, depending on which aspects you want password protected. System requires a password both to boot the system and to enter Setup. Setup requires a password only to enter Setup. A password may be at most 8 characters long.*

To Establish Password

1. Choose the Set Password option from the CMOS Setup Utility Main Menu and press <Enter>.
2. When you see Enter Password, enter the desired password and press <Enter>.
3. At the Confirm Password prompt, retype the desired password, then press <Enter>.
4. Select Save to CMOS and exit, type <Y>, then <Enter>.

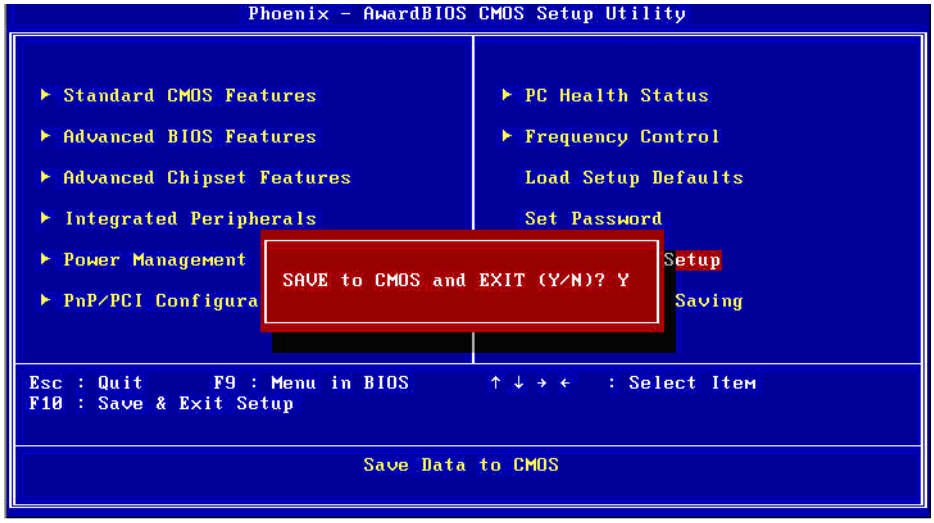
To Change Password

1. Choose the Set Password option from the CMOS Setup Utility main menu and press <Enter>.
2. When you see Enter Password, enter the existing password and press <Enter>.
3. You will see the Confirm Password prompt, type it in again, and press <Enter>.
4. Select Set Password again, and at the Enter Password prompt, enter the new password and press <Enter>.
5. At the Confirm Password prompt, retype the new password, and press <Enter>.
6. Select Save to CMOS and exit, type <Y>, then <Enter>.

To Disable a Password

1. Choose the Set Password option from the CMOS Setup Utility main menu and press <Enter>.
2. When you see the Enter Password prompt, enter the existing password and press <Enter>.
3. You will see Confirm Password, type it in again, and press <Enter>.
4. Select Set Password again, and at the Enter Password prompt, DO NOT enter anything - just press <Enter>.
5. At the Confirm Password prompt, again, DO NOT type in anything - just press <Enter>.
6. Select Save to CMOS and exit, type <Y>, then <Enter>.

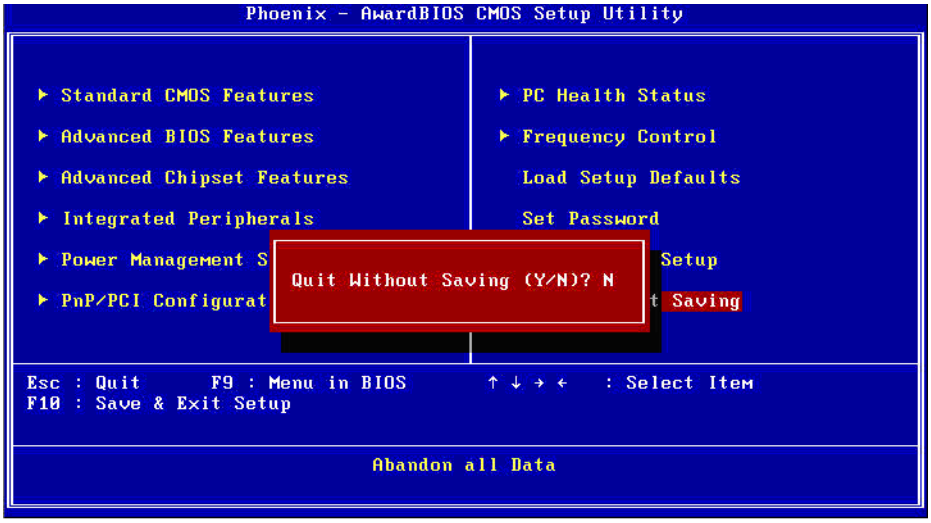
3.2.12 Save & Exit Setup



Note! *Typing <Y> will quit the BIOS Setup Utility and save the user setup values to CMOS.*

Typing <N> will return to BIOS Setup.

3.2.13 Quit Without Saving



Note! *Typing <Y> will quit the BIOS Setup Utility without saving any changes to CMOS.*

Typing <N> will return to the BIOS Setup Utility.

Chapter 4

S/W Introduction & Installation

4.1 S/W Introduction

The mission of Advantech Embedded Software Services is to "Enhance quality of life with Advantech platforms and Microsoft Windows® embedded technology." We enable Windows® Embedded software products on Advantech platforms to more effectively support the embedded computing community. Customers are freed from the hassle of dealing with multiple vendors (Hardware suppliers, System integrators, Embedded OS distributor) for projects. Our goal is to make Windows® Embedded Software solutions easily and widely available to the embedded computing community.

4.2 Driver Installation

4.2.1 Windows XP professional

To install the drivers for Windows XP Professional, insert the CD into the CD-Rom, it will auto-detect the hardware platform and then pop up with the “Embedded Computing Install Wizard” box; just select the drivers that you want to install then click “Install All Selected Drivers”. Follow the Driver Setup Wizard instructions; click "Next" to complete the installation.

4.2.2 Other OS

To install the drivers for Other Windows OS or Linux, please browse the CD to run the setup file under each chipset folder on the CD-ROM.

4.3 SUSI Application Library

4.3.1 SUSI Introduction

To make hardware easier and convenient to access for programmers, Advantech has released a suite of API (Application Programming Interface) in the form of a program library. The program Library is called Secured and Unified Smart Interface or SUSI for short.

In modern operating systems, user space applications cannot access hardware directly. Drivers are required to access hardware. User space applications access hardware through drivers. Different operating systems usually define different interface for drivers. This means that user space applications call different functions for hardware access in different operating systems. To provide a uniform interface for accessing hardware, an abstraction layer is built on top of the drivers and SUSI is such an abstraction layer. SUSI provides a uniform API for application programmers to access the hardware functions in different Operating Systems and on different Advantech hardware platforms.

Application programmers can invoke the functions exported by SUSI instead of calling the drivers directly. The benefit of using SUSI is portability. The same set of API is defined for different Advantech hardware platforms. Also, the same set of API is implemented in different Operating Systems including Windows XP and Windows CE. This user’s manual describes some sample programs and the API in SUSI. The hardware functions currently supported by SUSI can be grouped into a few categories including Watchdog, I^2C, SMBus, GPIO, and VGA control. Each category of API in SUSI is briefly described below.

4.3.2 SUSI Functions

4.3.2.1 The GPIO API

General Purpose Input/Output (GPIO) is a flexible parallel interface that allows a variety of custom connections, and supports digital I/O devices.

4.3.2.2 The I^2C API

I^2C is a bi-directional two-wire bus that was developed by Philips for use in their televisions in the 1980s and nowadays is used in various types of embedded systems. The strict timing requirements defined in the I^2C protocol has been taken care of by SUSI. Instead of asking application programmers to figure out the strict timing requirements in the I^2C protocol, the I^2C API in SUSI can be used to control I^2C devices by invoking other function calls. SUSI provides a consistent programming interface for different Advantech boards. That means user programs using SUSI are portable among different Advantech boards as long as the boards and SUSI provide the required functionalities. Overall product development times can be greatly reduced using SUSI.

4.3.2.3 The SMBus API

The System Management Bus (SMBus) is a two-wire interface defined by Intel ? Corporation in 1995. It is based on the same principles of operation of I^2C and is used in personal computers and servers for low-speed system management communications. Nowadays, it can be seen in many types of embedded systems. As with other API in SUSI, the SMBus API is available on many platforms including Windows XP and Windows CE.

4.3.2.4 The VGA Control API

There are two kinds of VGA control APIs, backlight on/off control and brightness control. Backlight on/off control allows a developer to turn on or off the backlight, and to control brightness smoothly.

4.3.2.5 The Watchdog API

A watchdog timer (abbreviated as WDT) is a hardware device which triggers an action, e.g. rebooting the system, if the system does not reset the timer within a specific period of time. The WDT API in SUSI provides developers with functions such as starting the timer, resetting the timer, and setting the timeout value if the hardware requires customized timeout values.

4.3.2.6 The Hardware Monitor API

The hardware monitor (abbreviated as HWM) is a system health supervision capability achieved by placing certain I/O chips along with sensors for inspecting the target of interests for certain condition indexes, such as fan speed, temperature and voltage etc.

However, due to the inaccuracy among many commercially available hardware monitoring chips, Advantech has developed a unique scheme for hardware monitoring - achieved by using a dedicated micro-processor with algorithms specifically designed for providing accurate, real-time and reliable data content; helping protect your system in a more reliable manner.

4.3.3 SUSI Installation

SUSI supports many different operating systems. Each subsection below describes how to install SUSI and related software on a specific operating system. Please refer to the subsection matching your operating system.

4.3.3.1 Windows XP

In windows XP, you can install the library, drivers and demo programs onto the platform easily using the installation tool - The SUSI Library Installer. After the installer has executed, the SUSI Library and related files for Windows XP can be found in the target installation directory. The files are listed in the following table.

Directory	Contents
\Library	■ Susi.lib Library for developing the applications on Windows XP. ■ Susi.dll Dynamic library for SUSI on Windows XP.
\Demo	■ SusiDemo.EXE Demo program on Windows XP. ■ Susi.dll Dynamic library for SUSI on Windows XP.
\Demo\SRC	Source code of the demo program on Windows XP.

The following section illustrates the installation process.

Note! *he version of the SUSI Library Installer shown on each screen shot below depends on your own particular version.*

1. Extract Susi.zip.
2. Double-click the "Setup.exe" file.

The installer searches for a previous installation of the SUSI Library. If it locates one, a screen shot opens asking whether you want to modify, repair or remove the software. If a previous version is located, please see the section of [Maintenance Setup]. If it is not located, the following screen shot opens. Click Next.

4.3.3.2 Windows CE

In windows CE, there are three ways to install the SUSI Library, you can install it manually or use Advantech CE-Builder to install the library or just copy the programs and the library onto a compact flash card.

Express Installation:

You can use Advantech CE-Builder to load the library into the image.

- First, you click the My Component tab.
- In this tab, you click Add New Category button to add a new category, eg. the SUSI Library.
- Then you can add a new file in this category, and upload the SUSI.dll for this category.
- After these steps, you can select the SUSI Library category you created for every project.

Manual Installation:

You can add the SUSI Library into the image by editing any bib file.

- First you open project.bib in the platform builder.
- Add this line to the MODULES section of project.bib
  Susi.dll $(_FLATRELEASEDIR)\Susi.dll NK SH
- If you want to run the window-based demo, add following line:
  SusiTest.exe $(_FLATRELEASEDIR)\SusiTest.exe
- If you want to run the console-based demo, add following lines:
  Watchdog.exe $(_FLATRELEASEDIR)\Watchdog.exe NK S
  GPIO.exe $(_FLATRELEASEDIR)\GPIO.exe NK S
  SMBUS.exe $(_FLATRELEASEDIR)\SMBUS.exe NK S
- Place the three files into any files directory.
- Build your new Windows CE operating system.

4.3.4 SUSI Sample Programs

4.3.4.1 Sample Programs

The sample programs demonstrate how to incorporate SUSI into your program. There are sample programs for two categories of operating system, i.e. Windows XP and Windows CE. The sample programs run in graphics mode in Windows XP and Windows CE. The sample programs are described in the subsections below.

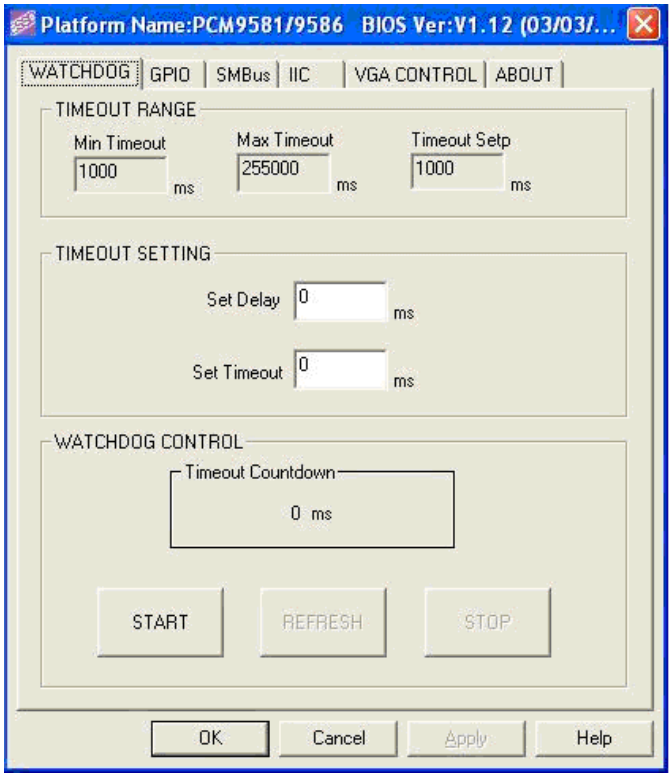
4.3.4.2 Windows Graphics Mode

There are sample programs of Windows in graphics mode for two categories of operating system, i.e. Windows CE and Windows XP. Each demo application contains an executable file SusiDemo.exe, a shared library Susi.dll and source code within the release package. The files of Windows CE and Windows XP are not compatible with each other.

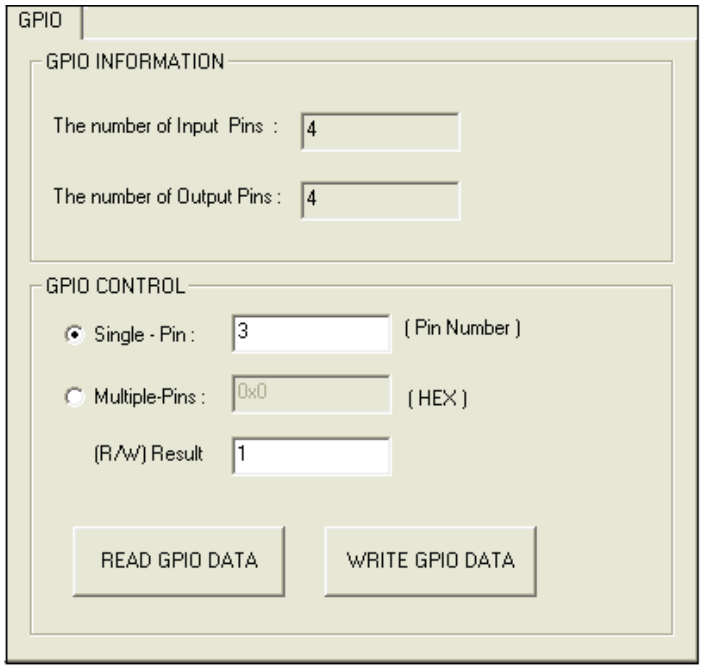
SusiDemo.exe is an executable file and it requires the shared library, Susi.dll, to demonstrate the SUSI functions. The source code of SusiDemo.exe also has two versions, i.e. Windows CE and Windows XP, and must be compiled under Microsoft Visual C++ 6.0 on Windows XP or under Microsoft Embedded Visual C++ 4.0 on Windows CE. Developers must add the header file Susi.h and library Susi.lib to their own projects when they want to develop something with SUSI.

4.3.4.3 SusiDemo.exe

The SusiDemo.exe test application is an application which uses all functions of the SUSI Library. It has five major function blocks: Watchdog, GPIO, SMBus, I^2C and VGA control. The following screen shot appears when you execute SusiDemo.exe. You can click function tabs to select test functions respectively. Some function tabs will not show on the test application if your platform does not support such functions. For a complete support list, please refer to Appendix A. We describe the steps to test all functions of this application.



4.3.4.4 GPIO

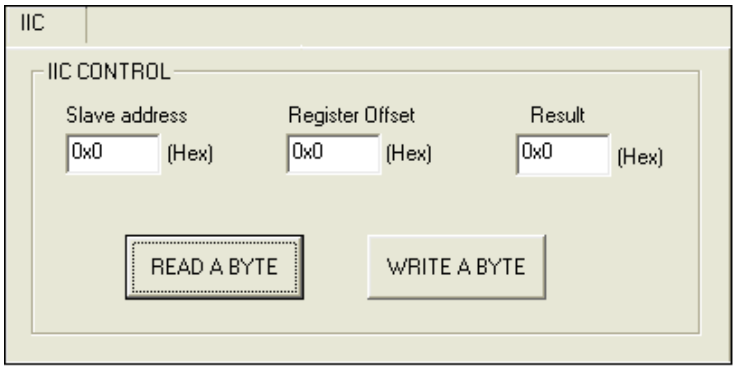


When the application is executed, it will display GPIO information in the GPIO INFORMATION group box. It displays the number of input pins and output pins. You can click the radio button to choose to test either the single pin function or multiple pin functions. The GPIO pin assignments of the supported platforms are located in Appendix B.

- **Test Read Single Input Pin**
  - Click the radio button- Single-Pin.
  - Key in the pin number to read the value of the input pin. The Pin number starts from '0'.
  - Click the READ GPIO DATA button and the status of the GPIO pin will be displayed in (R/W) Result field.
- **Test Read Multiple Input Pin**
  - Click the radio button- Multiple-Pins.
  - Key in the pin number from ‘0x01’ to ‘0x0F’ to read the value of the input pin. The pin numbers are ordered bitwise, i.e. bit 0 stands for GPIO 0, bit 1 stands for GPIO 1, etc. For example, if you want to read pin 0, 1, and 3, the pin numbers should be ‘0x0B’.
  - Click READ GPIO DATA button and the statuses of the GPIO pins will be displayed in (R/W) Result field.
- **Test Write Single Output Pin**
  - Click the radio button- Single-Pin.
  - Key in the pin numbers you want to write. Pin numbers start from '0'.
  - Key in the value either '0' or '1' in (R/W) Result field to write the output pin you chose above step.
  - Click the WRITE GPIO DATA button to write the GPIO output pin.

- **Test Write Multiple Output Pins**
  - Click the radio button- Multiple-Pins.
  - Key in the pin number from ‘0x01’ to ‘0x0F’ to choose the multiple pin numbers to write the value of the output pin. The pin numbers are ordered bitwise, i.e. bit 0 stands for GPIO 0, bit 1 stands for GPIO 1, etc. For example, if you want to write pin 0, 1, and 3, the pin numbers should be ‘0x0B’.
  - Key in the value in (R/W) Result field from ‘0x01’ to ‘0x0F’ to write the value of the output pin. The pin numbers are ordered bitwise, i.e. bit 0 stands for GPIO 0, bit 1 stands for GPIO 1, etc. For example, if you want to set pin 0 and 1 high, 3 to low, the pin number should be ‘0x0B’, and then you should key in the value ‘0x0A’ to write.
  - Click the WRITE GPIO DATA button to write the GPIO output pins.

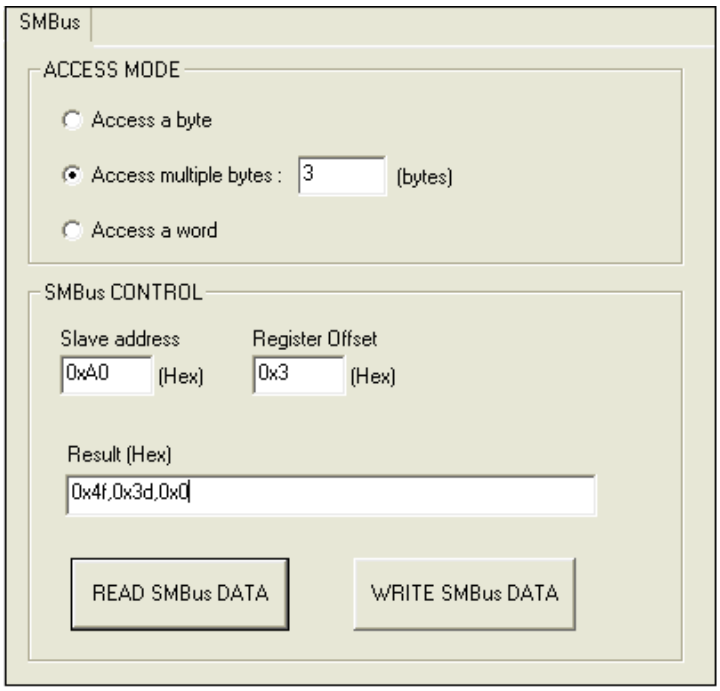
4.3.4.5 I²C



When the application is executed, you can read or write a byte of data through I²C devices. All data must be read or written in hexadecimal system.

- **Read a byte**
  - Key in the slave device address in Slave address field.
  - Key in the register offset in Register Offset field.
  - Click the READ A BYTE button and then a byte of data from the device will be shown on the Result field.
- **Write a byte**
  - Key in the slave device address in Slave address field.
  - Key in the register offset in Register Offset field.
  - Key in the desirous of data in Result field to write to the device.
  - Click the WRITE A BYTE button and then the data will be written to the device through I²C.

4.3.4.6 SMBus

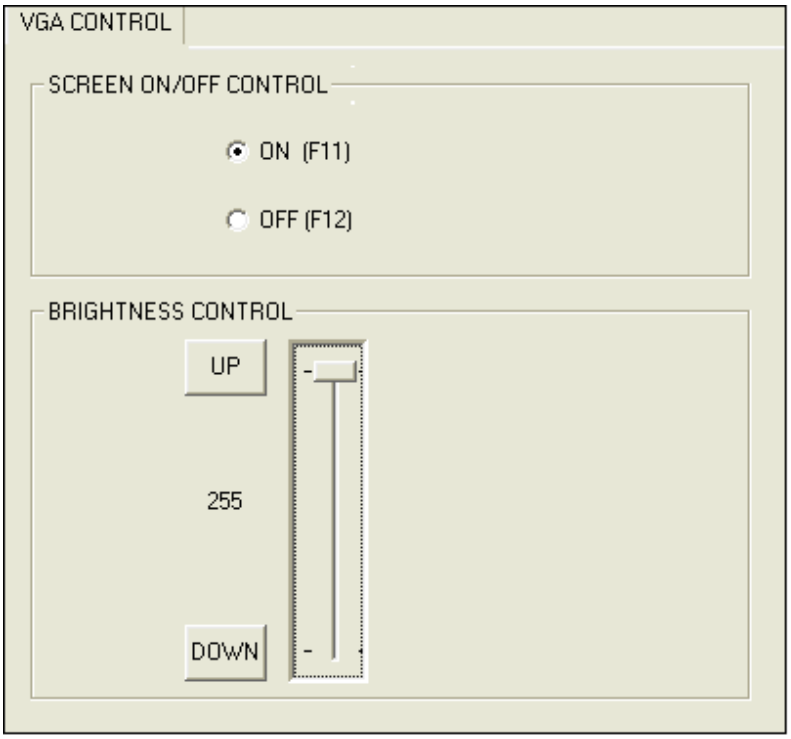


When the application has executed, you can click the radio button to choose to test each access mode, i.e. Access a byte, Access multiple bytes and Access a word. All data must be read or written in hexadecimal except the numbers for radio button: Access multiple bytes mode must be written in decimal. You can test the functionalities of the watchdog as follows:

- **Read a byte**
  - Click the radio button- Access a byte.
  - Key in the slave device address in the Slave address field.
  - Key in the register offset in the Register Offset field.
  - Click the READ SMBus DATA button and a byte of data from the device will be shown on the Result field.
- **Write a byte**
  - Click the radio button- Access a byte.
  - Key in the slave device address in Slave address field.
  - Key in the register offset in Register Offset field.
  - Key the desired data in the Result field to write to the device.
  - Click the WRITE SMBus DATA button and then the data will be written to the device through SMBus.
- **Read a word**
  - Click the radio button- Access a word.
  - Key in the slave device address in the Slave address field.
  - Key in the register offset in the Register Offset field.
  - Click the READ SMBus DATA button and then a word of data from the device will be shown on the Result field.

- **Write a word**
  - Click the radio button- Access a word.
  - Key in the slave device address in the Slave address field.
  - Key in the register offset in the Register Offset field.
  - Key in the desired data, such as 0x1234, in the Result field to write to the device.
  - Click the WRITE SMBus DATA button and the data will be written to the device through the SMBus.
- **Read Multiple bytes**
  - Click the radio button- Access multiple bytes.
  - Key in the slave device address in the Slave address field.
  - Key in the register offset in the Register Offset field.
  - Key in the desired number of bytes, such as 3, in the right side field of radio button- Access multiple bytes. The number must be written in decimal.
  - Click the READ SMBus DATA button and then all data from the device will be divided from each other by commas and be shown in the Result field.
- **Write Multiple bytes**
  - Click the radio button- Access multiple bytes.
  - Key in the slave device address in the Slave address field.
  - Key in the register offset in the Register Offset field.
  - Key in the desired number of bytes, such as 3, in the right side field of the radio button- Access multiple bytes. The number must be written in decimal.
  - Key in all the desired data in the Result field in hexadecimal format, divided by commas, for example, 0x50,0x60,0x7A.
  - Click the WRITE SMBus DATA button and all of the data will be written to the device through the SMBus.

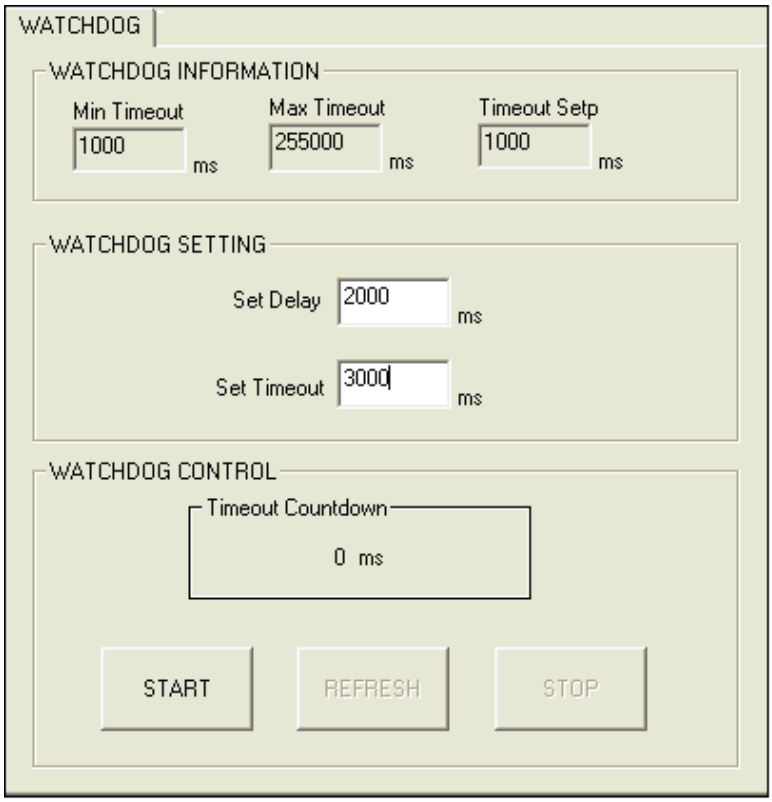
4.3.4.7 VGA Control



When the application is executed, it will display two blocks of VGA control functions. The application can turn on or turn off the screen shot freely, and it also can tune the brightness of the panels if your platform is being supported. You can test the functionalities of VGA control as follows:

- **Screen on/off control**
  - Click the radio button ON or push the key F11 to turn on the panel screen.
  - Click the radio button OFF or push the key F12 to turn off the panel screen.
  - The display chip of your platform must be in the support list in Appendix A, or this function cannot work.
- **Brightness control**
  - Move the slider in increments, using either the mouse or the direction keys, or click the UP button to increase the brightness.
  - Move the slider in decrements, using either the mouse or the direction keys, or click the DOWN button to decrease the brightness.

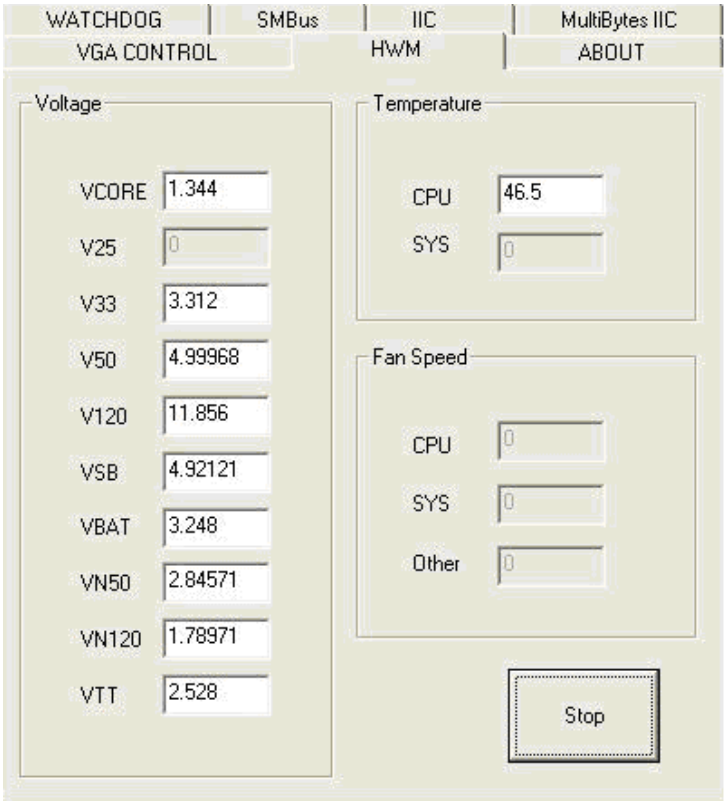
4.3.4.8 Watchdog



When the application is executed, it will display watchdog information in the WATCHDOG INFORMATION group box. It displays max timeout, min timeout, and timeout steps in milliseconds. For example, a 1~255 seconds watchdog will has 255000 max timeout, 1000 min timeout, and 1000 timeout steps. You can test the functionality of the watchdog as follows:

- Set the timeout value 3000 (3 sec.) in the SET TIMEOUT field and set the delay value 2000 (2 sec.) in the SET DELAY field, then click the START button. The Timeout Countdown field will countdown the watchdog timer and display 5000 (5 sec.).
- Before the timer counts down to zero, you can reset the timer by clicking the REFRESH button. After you click this button, the Timeout Countdown field will display the value of the SET TIMEOUT field.
- If you want to stop the watchdog timer, you just click the STOP button.

4.3.4.9 Hardware Monitor

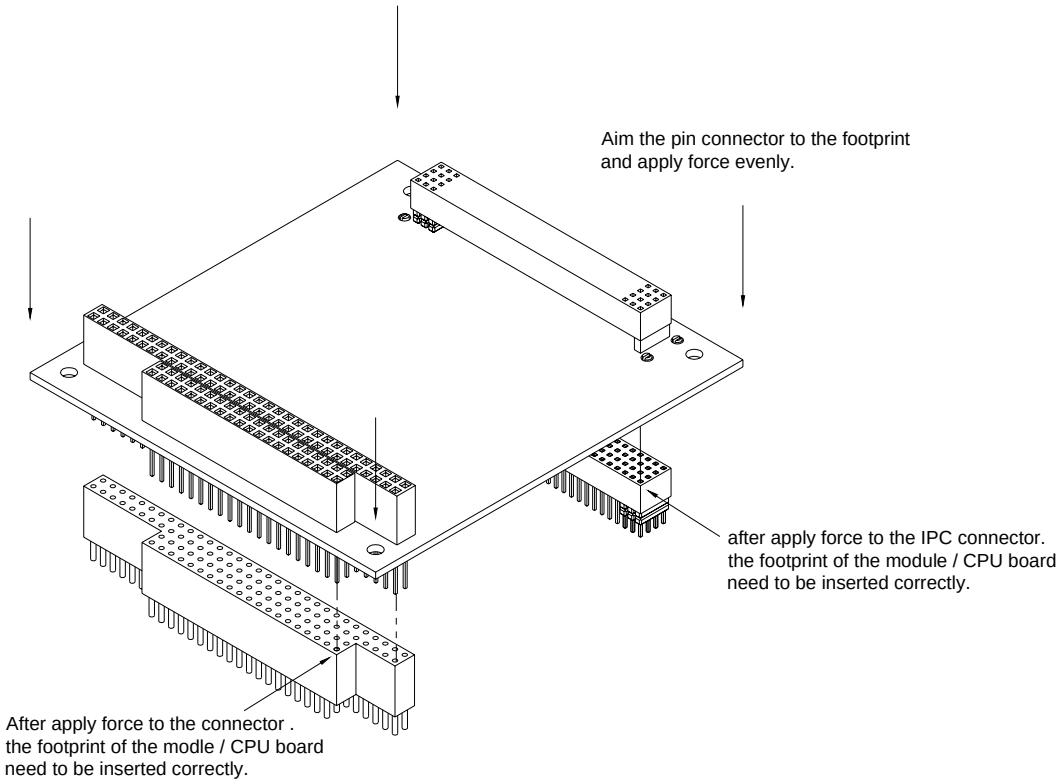


When the Monitor application is executed by clicking the button, hardware monitoring data values will be displayed. If certain data values are not supported by the platform, the correspondent data field will be grayed-out with a value of 0.

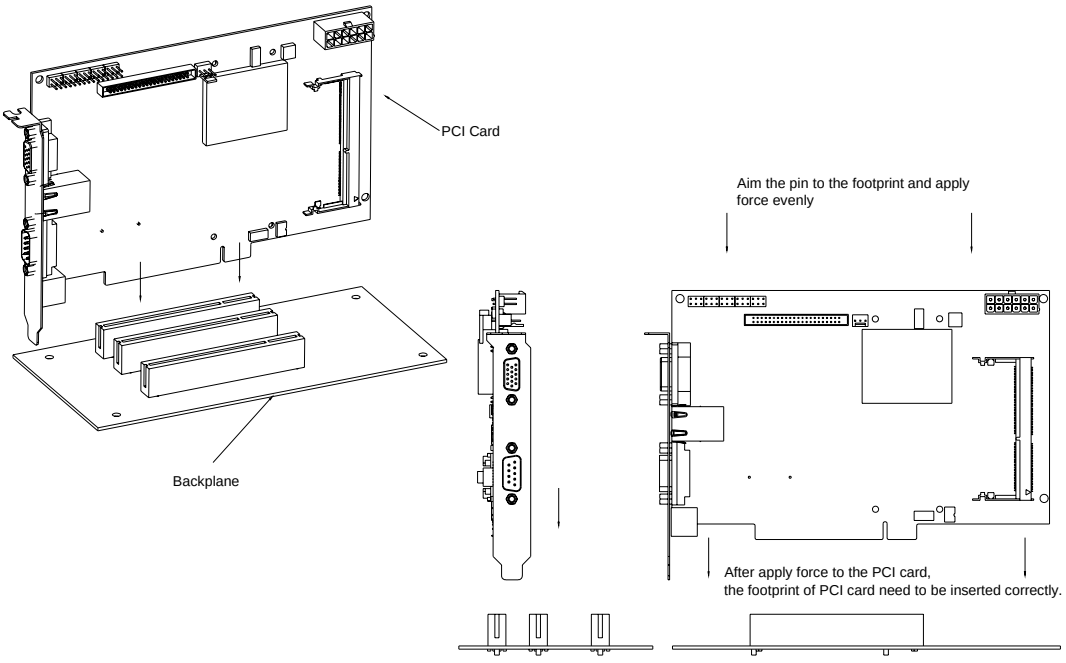
Chapter 5

Extension I/O Installation

5.1 PC-104


Aim the pin connector to the footprint
and apply force evenly.
after apply force to the IPC connector.
the footprint of the module / CPU board
need to be inserted correctly.
After apply force to the connector .
the footprint of the modle / CPU board
need to be inserted correctly.

5.2 PCI Riser Card


PCI Card
Backplane
Aim the pin to the footprint and apply
force evenly
After apply force to the PCI card,
the footprint of PCI card need to be inserted correctly.

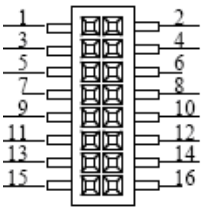
Appendix A

Pin Assignments

A.1 CN2: COM port 1/2 D-Sub Connector

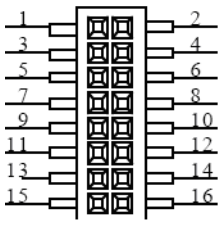
CN2	COM port 1/2 Connector			
Part Number	1654409101			
Footprint	DB9D-VM7MX2			
Description	D-SUB Conn. 18P DUAL PORT 90D(M) DIP			
Pin	**RS232**	**RS232**	**RS422**	**RS485**
1	DCD	DCD	TXD-	DATA-
2	SINA	SINA	TXD+	DATA+
3	SOUT	SOUT	RXD+	NC
4	DTR	DTR	RXD-	NC
5	GND	GND	GND	GND
6	DSR	DSR	NC	NC
7	RTS	RTS	NC	NC
8	CTS	CTS	NC	NC

A.2 CN7: VGA Connecter



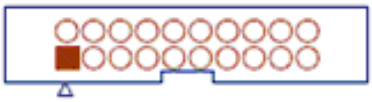
CN7	VAG Connector		
Part Number	**1653208260**		
Footprint	**BH8X2SV**		
Description	**Box HEADER 8*2P 180D (M) 2.00 mm**		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	DAC_L_R	O	
2	VCC_5V_CRT	PWR	+5V
3	DAC_L_G	O	
4	GND	GND	
5	DAC_L_B	O	
6	NC		
7	NC		
8	CRTDDC_L_D	I/O	
9	GND	GND	
10	DAC_L_HSYNC	O	
11	GND	GND	
12	DAC_L_VSYNC	O	
13	GND	GND	
14	CRTDDC_L_C	I/O	
15	VGA_ALW	GND	
16	NC		

A.3 CN8: Audio Connecter



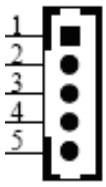
CN8	Audio Connecter		
Part Number	**1653208201**		
Footprint	**BH8X2DV-2M**		
Description	**BOX HEADER 8*2P 180D (M) 2.00 mm**		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	Speaker Out R+	OUT	+V5
2	Speaker Out R-	OUT	+V5
3	Speaker Out L+	OUT	+V5
4	Speaker Out L-	OUT	+V5
5	HPOUTR	OUT	
6	HPOUTL	OUT	
7	AGND	GND	
8	AGND	GND	
9	Line In Right	IN	
10	Line In Left	IN	
11	AGND	GND	
12	AGND	GND	
13	NC		
14	MIC2 In	IN	
15	MIC1 In	IN	
16	AGND	GND	

A.4 CN9: COM3/4 Connecter



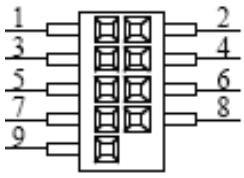
CN9	COM3/4 Connector		
Part Number	**1653210260**		
Footprint	**BH10X2SV**		
Description	**BOX HEADER 10*2P 180D (M) 2.0 mm SMD W/O Pb**		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	DCDC#	IN	
2	DSRC#	IN	
3	SINC	IN	
4	RTSC#	I/O	
5	SOUTC	OUT	
6	CTSC#	IN	
7	DTRC#	I/O	
8	RIC#	IN	
9	GND		
10	GND		
11	DCDD#	IN	
12	DSRD#	IN	
13	SIND	IN	
14	RTSD#	I/O	
15	SOUTD	OUT	
16	CTSD#	IN	
17	DTRD#	I/O	
18	RID#	IN	
19	GND		
20	GND		

A.5 CN10: IrDA Connecter



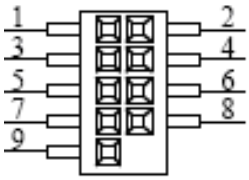
CN10	IrDA Connecter		
Part Number	**1655305020**		
Footprint	**WHL5V-2M**		
Description	**WAFER BOX 2.0 mm 5P 180D MALE W/LOCK**		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	VCC_5V_SIR	PWR	+5V
2	NC		
3	IRRX	IN	+5V
4	GND	GND	
5	IRTX	OUT	+5V

A.6 CN11: USB4/5 Connector



CN11	USB4/5 Connector		
Part Number	**1653205261**		
Footprint	**HD_5x2P_79_BOX_N10**		
Description	**PIN HEADER 5x2P 180D (M) 2.0 mm SMD IDIOT-PROOF**		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	VCC5_USB45	PWR	+5V
2	VCC5_USB45	PWR	+5V
3	C_USB_PN4	I/O	
4	C_USB_PN5	I/O	
5	C_USB_PP4	I/O	
6	C_USB_PP5	I/O	
7	GND		
8	GND		
9	GND		

A.7 CN12: USB2/3 Connector

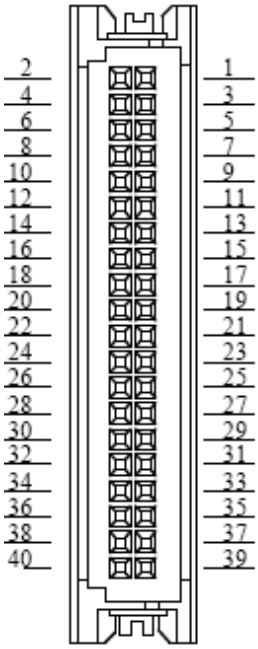


CN12	USB2/3 Connector		
Part Number	1653205261		
Footprint	HD_5x2P_79_BOX_N10		
Description	PIN HEADER 5x2P 180D (M) 2.0 mm SMD IDIOT-PROOF		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	VCC5_USB23	PWR	+5V
2	VCC5_USB23	PWR	+5V
3	C_USB_PN2	I/O	
4	C_USB_PN3	I/O	
5	C_USB_PP2	I/O	
6	C_USB_PP3	I/O	
7	GND		
8	GND		
9	GND		

A.8 CN13: PS2 Connecter

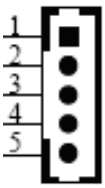
CN13	PS2 Connecter		
Part Number	1655306020		
Footprint	WHL6V-2M		
Description	WAFER BOX 2.0 mm 6P 180D (M) W/LOCK		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	KCK	IN	+5V
2	KDT	IN	+5V
3	MCK	IN	+5V
4	GND		
5	KBVCC	PWR	+5V
6	MDT	IN	+5V

A.9 CN14: LVDS Connecter



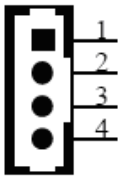
CN14	LVDS Connecter		
Part Number	**1653910261**		
Footprint	**SPH20X2A**		
Description	***CONN. SMD 10*2P 180D (M) DF13-20DP-1.25V**		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	VCC_LCD	PWR	+5V/+3.3V
2	VCC_LCD	PWR	+5V/+3.3V
3	GND		
4	GND		
5	LVDS0_N0	OUT	LVDS
6	LVDS0_P0	OUT	LVDS
7	GND		
8	LVDS0_N1	OUT	LVDS
9	LVDS0_P1	OUT	LVDS
10	GND		
11	LVDS0_N2	OUT	LVDS
12	LVDS0_P2	OUT	LVDS
13	GND		
14	LVDS0_C0N		
15	LVDS0_C0P		
16	GND		
17	LVDS0_N3		
18	LVDS1_N2		
19	GND		
20	GND		

A.10 CN15: Inverter Connecter



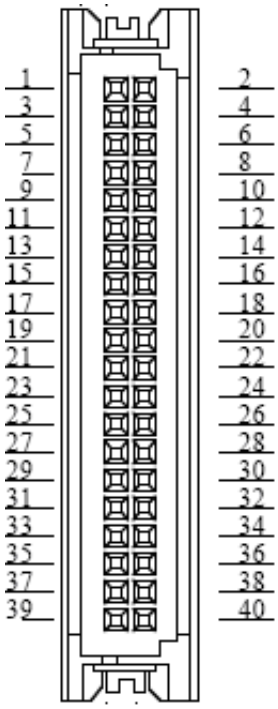
CN15	Inverter Connecter		
Part Number	1655305020		
Footprint	WHL5V-2M		
Description	WAFER BOX 2.0mm 5P 180D MALE W/LOCK		
Pin	Pin Name	Signal Type	Signal Level
1	VCC_INV_L	PWR	+12V
2	GND	GND	
3	LVDS_A_BKLTEN	OUT	+3.3V
4	VBR	OD	+3.3V
5	VCC_5V_L	PWR	+5V

A.11 CN16: CD in Connecter



CN16	CD In Connecter		
Part Number	1655304020		
Footprint	WF_4P_79_BOX_R1_D		
Description	WAFER BOX 2.0 mm 4P 180D (M) W/LOCK A2001WV2-4P		
Pin	Pin Name	Signal Type	Signal Level
1	CD_R	IN	
2	CDGND	GND	
3	CDGND	GND	
4	CD_L	IN	

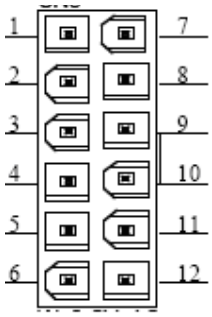
A.12 CN17: TTL Connecter



CN17	TTL Connecter		
Part Number	1653920200		
Footprint	SPH20X2		
Description	CONN. 20*2P 90D 1.25Mmm SMD WO/PB DF13-40DP-1.25V HRS		
Pin	Pin Name	Signal Type	Signal Level
1	VCC_LCD	PWR	+5V/+3.3V
2	VCC_LCD	PWR	+5V/+3.3V
3	GND		
4	GND		
5	VCC_LCD	PWR	+5V/+3.3V
6	VCC_LCD	PWR	+5V/+3.3V
7	DSTN_Vcon		
8	GND		
9	LD0	OUT	TTL
10	UD0	OUT	TTL
11	LD1	OUT	TTL
12	UD1	OUT	TTL
13	LD2	OUT	TTL
14	UD2	OUT	TTL
15	LD3	OUT	TTL
16	UD3	OUT	TTL
17	LD4	OUT	TTL
18	UD4	OUT	TTL
19	LD5	OUT	TTL
20	UD5	OUT	TTL

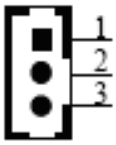
21	LD6	OUT	TTL
22	UD6	OUT	TTL
23	LD7	OUT	TTL
24	UD7	OUT	TTL
25	LD8	OUT	TTL
26	UD8	OUT	TTL
27	LD9	OUT	TTL
28	UD9	OUT	TTL
29	LD10	OUT	TTL
30	UD10	OUT	TTL
31	LD11	OUT	TTL
32	UD11	OUT	TTL
33	GND		
34	GND		
35	SHCLK	OUT	TTL
36	FLM	OUT	TTL
37	M/DE		
38	LOAD	OUT	TTL
39	NA		
40	ENVEE	OUT	

A.13 CN20: Power Connecter



CN5	Power Connecter		
Part Number	**1655412090**		
Footprint	**ATXCON-2X6V-42**		
Description	**Power CONN.6*2P 180D (M) DIP W/Fixed Lock**		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	GND	GND	
2	+5V	PWR	+5V
3	+5V	PWR	+5V
4	GND	GND	
5	+5V	PWR	+5V
6	+5V	PWR	+5V
7	GND	GND	
8	GND	GND	
9	+5VSB	PWR	+5V
10	PSON#	IN	+3.3V
11	GND	GND	
12	+12V	PWR	+12V

A.14 CN21: -V5 and -V12 Connecter

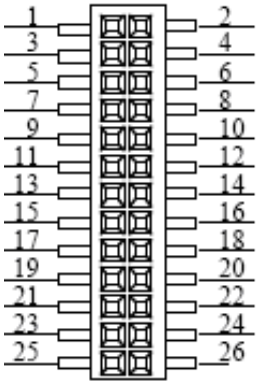


CN21	-5V&-12V Connecter		
Part Number	**1655303020**		
Footprint	**WHL3V-2M**		
Description	**WAFER BOX 2.0mm 3P 180D w/LOCK**		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	VCC5N	PWR	-5V
2	GND		
3	V12N	PWR	-12V

A.15 CN26: Panel Connector

CN26	HDD LED and POWER LED		
Part Number	1653007260		
Footprint	BH7X2SV		
Description	PIN HEADER SMD 2*7P 180D (M) P=2.0 mm		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	HDLEDA#	PWR	5V
2	HDD_LEDC#	I/O	
3	LED_POWER	PWR	5V
4	GND		
5	SUSLED	I/O	
6	GND		
7	LEDP_ACT	PWR	3.3V
8	ACTLED	IN	
9	LEDP_LNK	PWR	3.3V
10	LINKLED	IN	
11	FP_PSIN	OUT	3.3V
12	GND		
13	GND		
14	MASTER_RESET#	OUT	

A.16 CN28: LPT Connecter

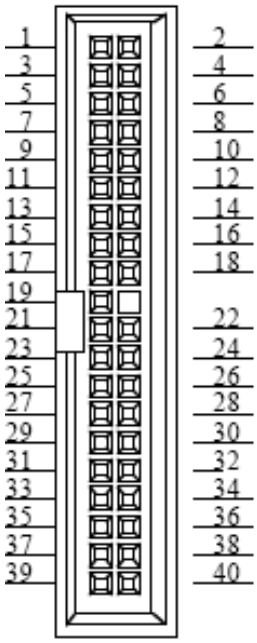


CN28	LPT Connecter	
Part Number	**1653213204**	
Footprint	**BH13X2DV-2M**	
Description	**BOX HEADER 13*2P 180D (M) 2.0 mm DIP WO/PB**	
Pin	**Pin Name (LPT)**	**Signal Level**
1	PPT_STB#	
2	PPT_AFD#	
3	PPT_PD0	
4	PPT_ERR#	
5	PPT_PD1	
6	PPT_INIT#	
7	PPT_PD2	
8	PPT_SLIN#	
9	PPT_PD3	
10	GND	
11	PPT_PD4	
12	GND	
13	PPT_PD5	
14	GND	
15	PPT_PD6	
16	GND	
17	PPT_PD7	
18	GND	
19	PPT_ACK#	
20	GND	
21	PPT_BUSY	
22	GND	
23	PPT_PE	
24	GND	
25	PPT_SLCT	
26	NC	

A.17 FAN1/2: FAN Connector

FAN1/2	FAN Connector		
Part Number	**1655303020**		
Footprint	**WHL3V-2M**		
Description	**WAFER BOX 2.0 mm 3P 180D w/LOCK**		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	FAN_DET	OUT	
2	VCC_FAN	PWR	5V
3	GND		

A.18 CN24/25: IDE Connecter



CN24/25	IDE Connecter		
Part Number	**1653222262**		
Footprint	**BH22X2SV**		
Description	**BOX HEADER SMD 22*2P 180D (M) 2.00 mm IDIOT-PROOF**		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	RESET#	Out	+5V
2	GND	GND	
3	DD7	I/O	+5V
4	DD8	I/O	+3.3V
5	DD6	I/O	+5V
6	DD9	I/O	+5V
7	DD5	I/O	+5V
8	DD10	I/O	+5V

9	DD4	I/O	+5V
10	DD11	I/O	+5V
11	DD3	I/O	+5V
12	DD12	I/O	+5V
13	DD2	I/O	+5V
14	DD13	I/O	+5V
15	DD1	I/O	+5V
16	DD14	I/O	+5V
17	DD0	I/O	+5V
18	DD15	I/O	+5V
19	GND	GND	
21	DMARQ	Out	+5V
22	GND	GND	
23	DIOW#	Out	+5V
24	GND	GND	
25	DIOR#	Out	+5V
26	GND	GND	
27	IORDY	Out	+5V
28	CSEL	Out	+5V
29	DMACK#	Out	+5V
30	GND	GND	
31	INTRQ	In	+5V
32	NC		
33	DA1	In	+5V
34	PDIAG#	In	+5V
35	DA0	In	+5V
36	DA2	In	+5V
37	CS#1	Out	+5V
38	CS#3	Out	+5V
39	DASP#	Out	+5V
40	GND	GND	
41	VCC5	PWR	+5V
42	VCC5	PWR	+5V
43	GND		
44	NA		

A.19 CN18: PC104 Connecter

CN18	**PC-104 Connector**
Part Number	**165313222A, 165312022A**
Footprint	**PCI-PLUS**
Description	**PCB SKT 32*2 180D(F)H=11.54**

A.20 CN22: CF TYPEII Connecter

CN22	CF TYPEII Connecter		
Part Number	**1653003278**		
Footprint	**COMPACK-T12**		
Description	**CF 50P 90D(M)SMD TypeII N7E50-H516CES70004-DY**		
Pin	**Pin Name**	**Signal Type**	**Signal Level**
1	GND	GND	
2	IDE_SDD3	I/O	+5V
3	IDE_SDD4	I/O	+5V
4	IDE_SDD5	I/O	+5V
5	IDE_SDD6	I/O	+5V
6	IDE_SDD7	I/O	+5V
7	IDE_SDCS#1	OUT	
8	GND	GND	
9	GND	GND	
10	GND	GND	
11	GND	GND	
12	GND	GND	
13	+5V	PWR	+5V
14	GND	GND	
15	GND	GND	
16	GND	GND	
17	GND	GND	
18	IDE_SDA2	IN	+5V
19	IDE_SDA1	IN	+5V
20	IDE_SDA0	IN	+5V
21	IDE_SDD0	I/O	+5V
22	IDE_SDD1	I/O	+5V
23	IDE_SDD2	I/O	+5V
24	NC		
25	GND	GND	
26	NC		
27	IDE_SDD11	I/O	+5V
28	IDE_SDD12	I/O	+5V
29	IDE_SDD13	I/O	+5V
30	IDE_SDD14	I/O	+5V
31	IDE_SDD15	I/O	+5V
32	IDE_SDCS#3	OUT	+5V
33	NC		
34	IDE_SDIOR#	OUT	+5V
35	IDE_SDIOW#	OUT	+5V
36	IDE_WE#	OUT	+5V
37	IDE_IRQ	IN	+5V
38	+5V	PWR	+5V
39	CF_CSEL#	OUT	GND

40	NC		
41	RESET#	OUT	+5V
42	IDE_SDIORDY	OUT	+5V
43	IDE_SDDREQ	OUT	+5V
44	IDE_SDDACK#	OUT	+5V
45	IDE_SDACTIVE#	I/O	+5V
46	IDE_SATADET	IN	+5V
47	IDE_SDD8	I/O	+5V
48	IDE_SDD9	I/O	+5V
49	IDE_SDD10	I/O	+5V
50	GND		

A.21 DIMM1: DDR SODIMM Socket

DIMM1	**DDR SODIMM Socket**
Part Number	**16515A0995**
Footprint	**DDR-SODIMM-STD65**
Description	**SKT DIMM 200P DDR 0.6 mm H=5.2 mm SMD WO/Pb**

A.22 PCI1/2: PCI Connector

PCI1/2	**PCI Connector**
Part Number	**16542C0200**
Footprint	**PCI-SL**
Description	**SLOT 60*2P 180D (F) DIP WO/Pb**

Appendix B

Optional Extras for the POD-6552

The POD-6552 requires several cables for normal operation. You can make them yourself or purchase an optional cable kit assembly, which includes the following.

B.1 PCM-10586-6552E Cable kit for POD-6552 A2

Part No.	Cable Description	POD-6552 Connector	Terminating Connector
1700000101	USB Cable	CN11, 12	10P 2.0 mm/USB 60 cm
1700001166	COM3, 4 Cable	CN9	20P 2.0 mm
1700001296	VGA Cable	CN7	15P to 16P 2.0 mm D-SUB L: 15 cm
1700160160	Audio Cable	CN8	16Pin (2.0 mm) L: 16 cm
1700260250	Parallel Port	CN28	25P to 26P 2.0 mm L: 25 cm
1701340603	Floppy Cable	CN27	34P FC34/34/Housing 34 Idiot-Proof L: 60 cm
1701440350	HDD Cable	CN24, 25	44P Gray IDC44P/IDC44P/IDC44P L: 35 cm
1701440500	HDD Cable	CN24, 25	40P Gray IDC40P/40P/Housing 44P L: 50 cm
1703080101	Power Cable	CN20	Wire 7P/Big 4P*2 L: 10 cm
1703060053	PS/2 KB & MOUSE	CN13	6P (MINI-DIN)-6P (Wafer 2.0 mm) L: 5 cm
1700060202	PS/2 KB & MOUSE		6P-6P-6P L: 20 cm

Appendix C

Watchdog Timer

C.1 Watchdog Timer

```
    ;The SCH3114/SCH3106 Runtime base I/O address is 800h
    ;Setting WatchDog time value location at offset 66h
    ;If set value "0", it is mean disable WatchDog function.
    Superio_GPIO_Port = 800h
    mov   dx,Superio_GPIO_Port + 66h
    mov   al,00h
    out   dx,al

.model small
            .486p
            .stack 256
            .data
            SCH3114_IO   EQU   800h
            .code
            org     100h
 .STARTup
;================================================
;47H
;enable WDT function bit [3:2]=11
;================================================

            mov   dx,SCH3114_IO + 47h
            mov   al,0ch
            out   dx,al

;================================================
;65H
;bit [1:0]=Reserved
;bit [6:2]Reserve=00000
;bit [7] WDT time-out Value Units Select
;Minutes=0 (default) Seconds=1
;================================================

            mov   dx,SCH3114_IO + 65h ;
            mov   al,080h
            out   dx,al

;================================================
;66H
;WDT timer time-out value
;bit[7:0]=0~255
;================================================

            mov   dx,SCH3114_IO + 66h
```

```
            mov   al,01h
            out   dx,al

;=================================================
;bit[0] status bit R/W
;WD timeout occurred =1
;WD timer counting = 0
;=================================================

            mov   dx,SCH3114_IO + 68h
            mov   al,01h
            out   dx,al
            .exit
             END
```

Appendix D

System Assignment

D.1 System I/O Ports

Table D.1: System I/O Ports

Addr. Range (Hex)	Device
00®C0F	Master DMA Controller
20®C21F	Master Interrupt Controller
2E®C2F	Configuration Index/Data
40®C5F	Timer/Counter
60®C6F	Keyboard Controller
60h	KBC Data
61h	Misc Funtions & Spkr Ctrl
64h	KBC Command/Status
70-77	RTC/COMS/NMI-Disable
78-7F	-available for system use-
80	-reserved-(debug port)
81-8F	DMA Page Registers
90-91	-available for system use-
92	System Control
93-9F	-available for system use-
A0-A1H	Slave Interrupt Controller
C0-DF	Slave DMA Controller
E0-FF	-available for system use-
100-1EF	-available for system use-
170-178	Secondary IDE Control
1F0-1F8	Primary IDE Control
200-20F	Game Port
2E8-2EF	COM4
2E0-2E7	COM2
378-37F	Parallel Port(standard & AFF)
3C0-3CF	EGA
3D0-2DF	VGA
3E8-3EF	COM3
3F0-2F7	Floppy Controller
3F8-3FF	COM1
778-77A	Parallel Port(ECP Extensions)(Port 378+400)
870-871	Hardware Monitor
800h-87Fh	Super IO runtime register
CF8-CFB	PCI Configuration Address
CFC-CFF	PCI Configuration Data
D00-FFFF	-available for system use-

D.2 1st MB memory map

Table D.2: 1st MB memory map	
Addr. Range (Hex)	**Device**
F0000h-FFFFFh	System ROM
D0000h-EFFFFh	Unused(reserved for Ethernet ROM)
C0000h-CFFFFh	Expansion ROM(for VGA BIOS)
B8000h-BFFFFh	CGA/EGA/VGA text
B0000h-B7FFFH	Unused
A0000h-AFFFFh	EGA/VGA graphics
00000h-9FFFFh	Base memory

D.3 DMA channel assignments

Table D.3: DMA channel assignments	
Channel	**Function**
0	Available
1	Available (audio)
2	Floppy disk (8-bit transfer)
3	Available (parallel port)
4	Cascade for DMA controller 1
5	Available
6	Available
7	Available

D.4 Interrupt assignments

Table D.4: Interrupt assignments

Interrupt#	Interrupt source
IRQ0	Interval timer
IRQ1	Keyboard
IRQ2	Interrupt from controller 2 (cascade)
IRQ3	COM2
IRQ4	COM1
IRQ5	COM4
IRQ6	FDD
IRQ7	LPT1
IRQ8	RTC
IRQ9	Reserved(audio)
IRQ10	COM3
IRQ11	Reserved for watchdog timer
IRQ12	PS/2 Mouse
IRQ13	INT from Co-processor
IRQ14	Primary IDE
IRQ15	Secondary IDE for CFC

Appendix E

Electrical Specifications

E.1 Input Power

This chapter describes how to choose a suitable power supply for this board. The guideling is as follows.

E.1.1 Power Supply Selection

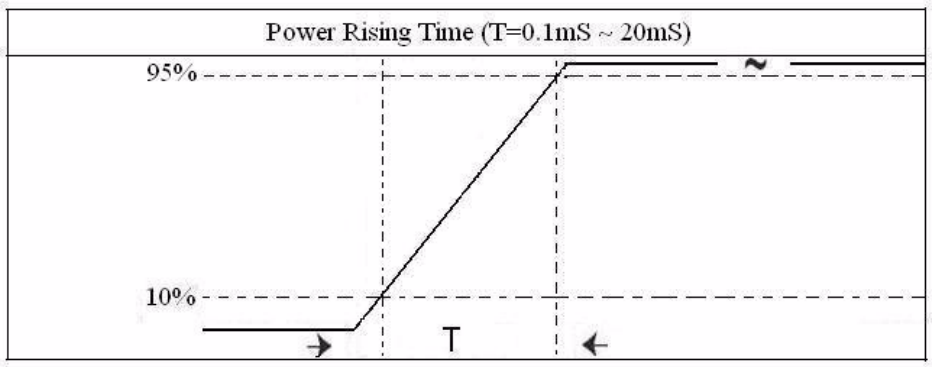
The power supply which we select should have over-current protection and the over-current protection value of the power supply must meet 1.5 ~ 2 times of the total power consumption.

E.1.2 Power Requirement of Power Supply

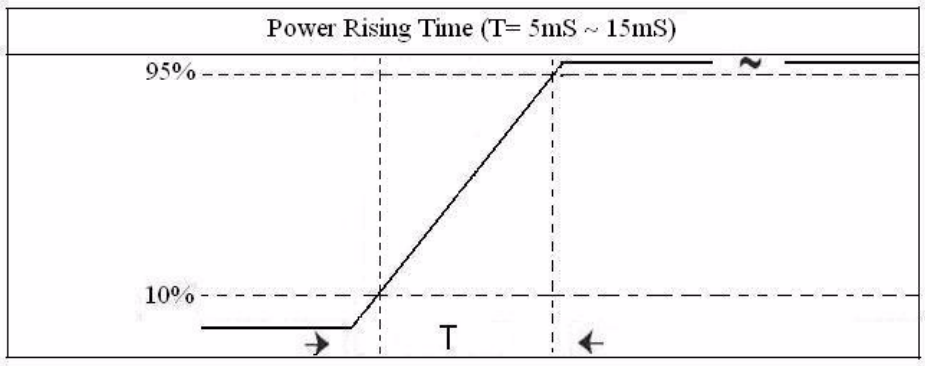
When trying to find a suitable power supply, consider not only this board power consumption but you also need to consider the total system power requirements. The power requirement is based on system configuration. For example, total power requirement = CPU board + peripheral (USB) + system device (IDE, SATA HD) + add on card.

E.1.3 Rising Time

1. ATX: Power Rising Time (T=0.1 mS ~ 20 mS)



2. AT: Power Rising Time (T=5 mS ~ 15 mS)



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